

## Fractional-N Clock Synthesizer and Multiplier

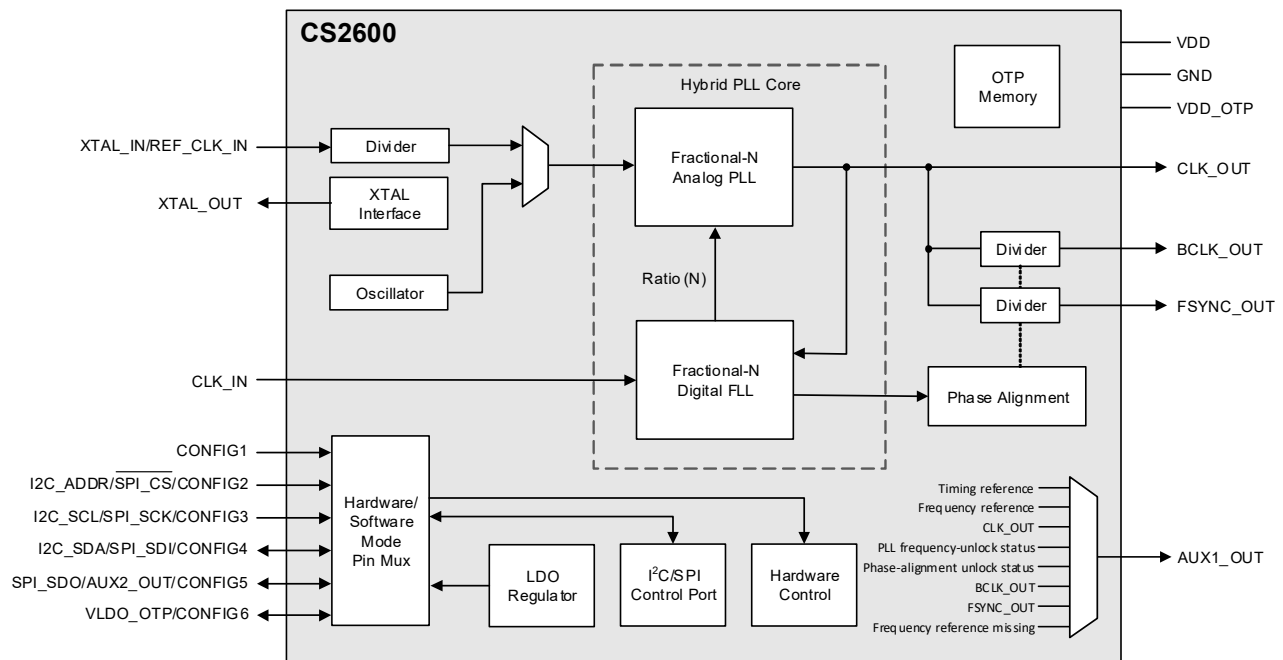
### Features

- Clock frequency synthesizer incorporating delta-sigma fractional-N analog PLL
  - Generates low-jitter 6–75 MHz clock (CLK\_OUT) from 8–75 MHz timing reference (REF\_CLK\_IN)
- Fractional clock multiplier and jitter reduction using hybrid analog/digital PLL
  - Generates low-jitter 6–75 MHz clock (CLK\_OUT), synchronized to a 50 Hz–30 MHz low-quality or intermittent frequency reference (CLK\_IN)
- Flexible timing reference source
  - External clock, external crystal, or built-in oscillator
- High resolution PLL ratio (1 PPM)
- 40 ps<sub>RMS</sub> period jitter (external timing reference), 35 ps<sub>RMS</sub> period jitter (oscillator reference)
- Glitchless clock output generated from intermittent input
- BCLK and FSYNC outputs (derived from CLK\_OUT) for digital audio applications
  - Phase alignment with CLK\_IN frequency reference

- Automatic rate control (ARC) for digital audio applications
  - Seamless transitions through changes in CLK\_IN frequency reference
- Customer-programmable startup configuration, using integrated one-time programmable (OTP) memory
- Hardware and software control modes
  - I<sup>2</sup>C/SPI control port
  - Hardware control with no host processor required
- Configurable auxiliary clock/status output
- Minimal board space required
  - No external analog loop-filter components
- Single-supply operation at 1.8 V or 3.3 V

### Applications

- Automotive audio systems
- Digital audio systems
- Network and USB audio interfaces
- IoT sensor and transducer systems
- Embedded systems



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## General Description

The CS2600 is a system-clocking device incorporating a programmable phase-locked loop (PLL). The hybrid analog/digital PLL architecture comprises a delta-sigma fractional-N analog PLL and a digital frequency-locked loop (FLL). The CS2600 enables frequency synthesis and clock generation from a stable timing reference clock. The device can generate low-jitter clocks from a noisy clock reference at frequencies as low as 50 Hz. An internal oscillator can provide the timing reference clock, enabling a reduction in external component requirements. The CS2600 can be configured using a control interface supporting I<sup>2</sup>C and SPI modes of operation. The device can also be configured in Hardware Control Mode using pull-up/pull-down resistors, reducing system software overhead.

The CS2600 supports BCLK and FSYNC outputs, derived from the PLL output signal. All of the clock outputs can be phase-aligned with the clock input source. The automatic rate control (ARC) function detects the clock input frequency and configures the PLL ratio for the required output. The ARC supports seamless transitions through changes in the reference frequency; the BCLK and FSYNC outputs are automatically adjusted to maintain the applicable ratios.

The CS2600 provides a built-in OTP memory to configure the default operating settings, loaded at boot-up. The OTP memory is optimized and managed to support multiple programming cycles.

The CS2600 can be powered from a single 1.8 V or 3.3 V supply. The device combines high performance with low power consumption.

The CS2600 is available in commercial-grade 16-pin QFN package for operation from –40°C to +85°C. The device is also available in the AEC-Q100-qualified grade-2 package for operation from –40°C to +105°C. See [Section 11](#) for ordering information.

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# 1 Pin Assignments and Descriptions

These sections show pin assignments and describe pin functions.

## 1.1 QFN Pin Assignments (Top View, Through Package)

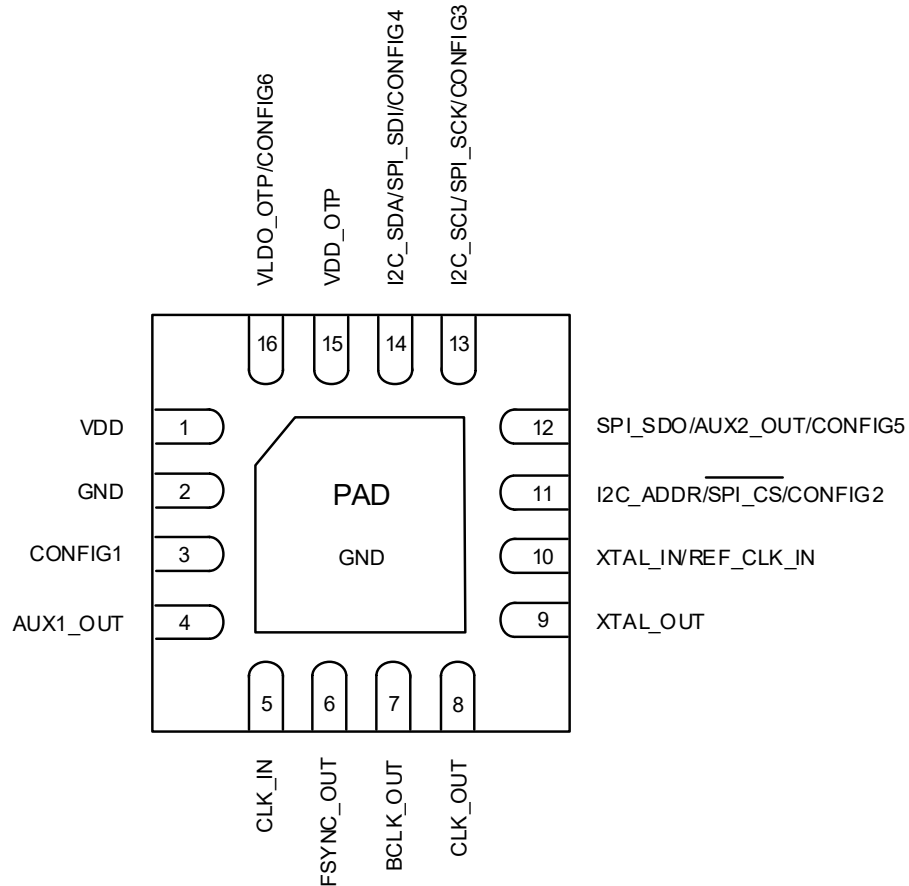


Figure 1-1. QFN 16-Pin Diagram (Top View, Through-Package)

## 1.2 Pin Descriptions

Table 1-1. Pin Descriptions

| Pin Name  | Pin #  | Power Supply | I/O | Description  |
|-----------|--------|--------------|-----|--|
| VDD       | 1      | —            | —   | <b>Power Supply.</b> 3.3 V/1.8 V supply for the digital and analog blocks.   |
| GND       | 2, PAD | —            | —   | <b>Ground and Pad.</b> The paddle must be connected to ground plane directly underneath the CS2600.                        |
| CONFIG1   | 3      | VDD          | I   | <b>Hardware Configuration 1.</b> Hardware Control Mode configuration connection. Connect to GND for Software Control Mode. |
| AUX1_OUT  | 4      | VDD          | O   | <b>Auxiliary Output.</b> Configurable clock output or status output.   |
| CLK_IN    | 5      | VDD          | I   | <b>Clock Input.</b> Frequency reference input for the digital FLL.   |
| FSYNC_OUT | 6      | VDD          | O   | <b>FSYNC Output.</b> PLL frame sync clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.                |
| BCLK_OUT  | 7      | VDD          | O   | <b>BCLK Output.</b> PLL bit clock output (CLK_OUT derived), which can be phase-aligned with CLK_IN.                        |
| CLK_OUT   | 8      | VDD          | O   | <b>Clock Output.</b> PLL clock output.   |

**Table 1-1. Pin Descriptions (Cont.)**

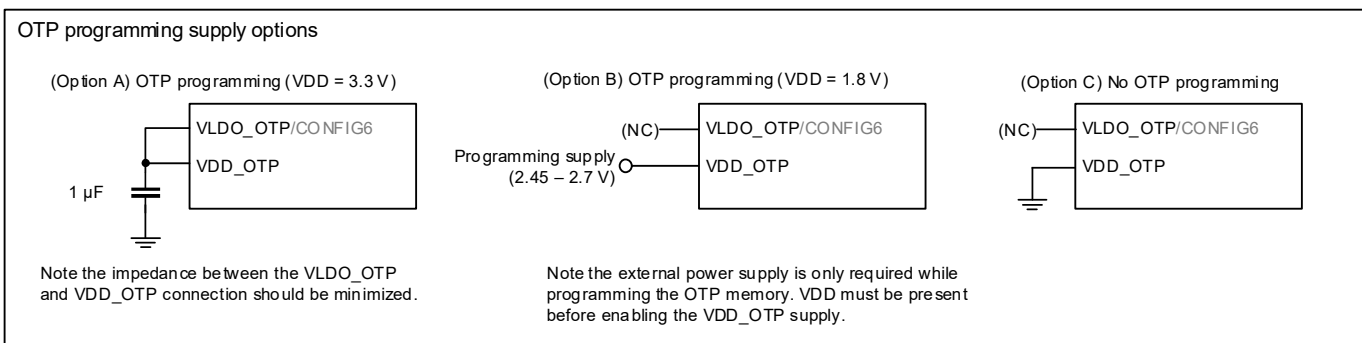
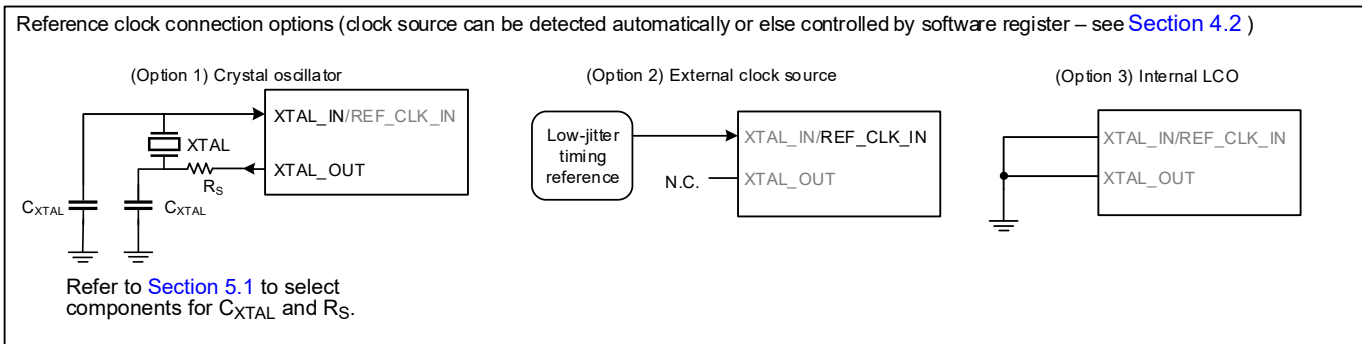
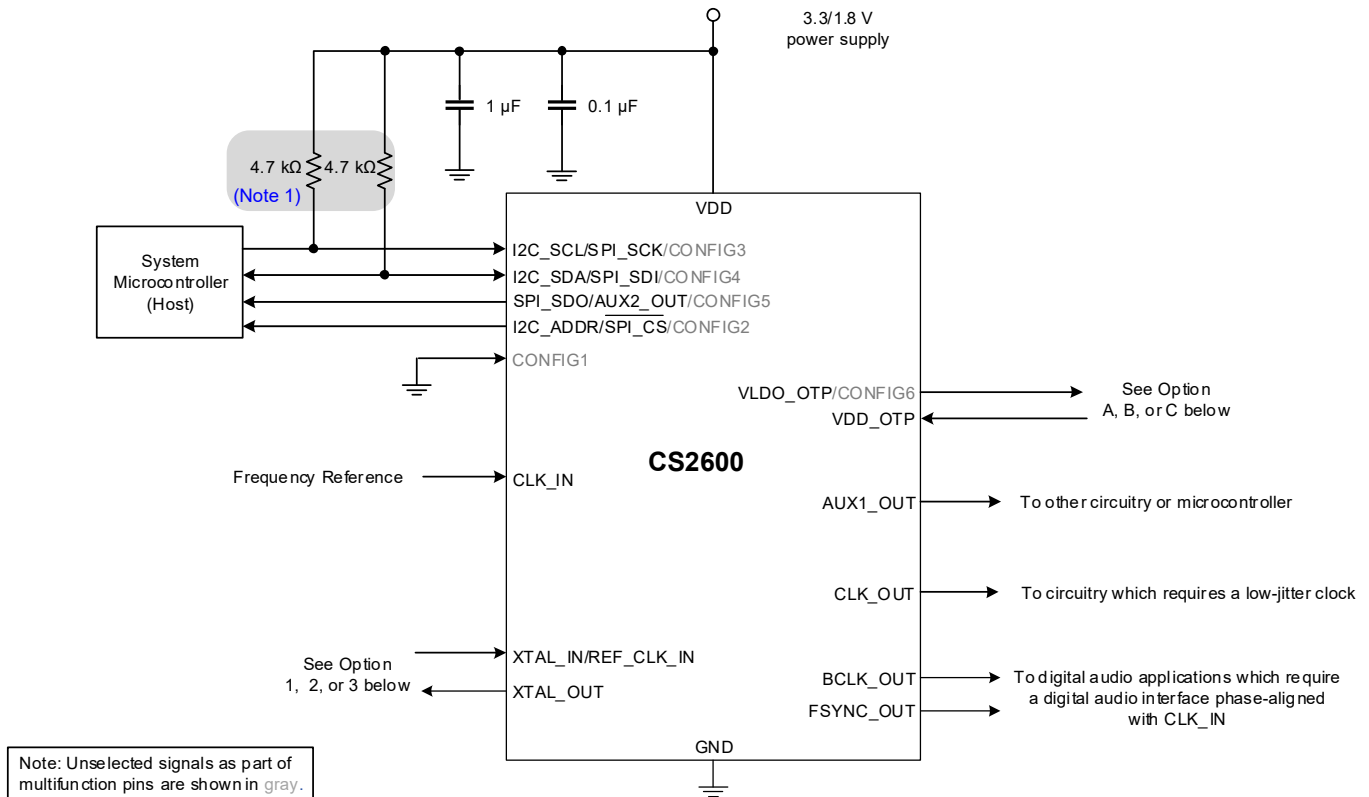
| Pin Name                 | Pin # | Power Supply | I/O | Description  |
|--------------------------|-------|--------------|-----|--|
| XTAL_OUT                 | 9     | VDD          | O   | <b>Crystal Connection.</b> Output for an external crystal. Connect to GND for internal oscillator reference clock.   |
| XTAL_IN/REF_CLK_IN       | 10    | VDD          | I   | <b>Crystal Connection.</b> Input for an external crystal.<br><b>Reference Clock.</b> External low-jitter timing reference clock input. Connect to GND for internal oscillator reference clock.   |
| I2C_ADDR/SPI_CS/CONFIG2  | 11    | VDD          | I   | <b>I2C Control-Port Address.</b> Chip address input for the I2C interface.<br><b>SPI Control-Port Chip Select.</b> Active-low chip select input for the SPI interface.<br><b>Hardware Configuration 2.</b> Hardware Control Mode configuration connection. |
| SPI_SDO/AUX2_OUT/CONFIG5 | 12    | VDD          | I/O | <b>SPI Control-Port Serial Data Out.</b> SPI data output.<br><b>Auxiliary Output 2.</b> Configurable status output.<br><b>Hardware Configuration 5.</b> Hardware Control Mode configuration connection.  |
| I2C_SCL/SPI_SCK/CONFIG3  | 13    | VDD          | I   | <b>I2C Control-Port Clock.</b> Clock input for the I2C interface.<br><b>SPI Control-Port Clock.</b> Clock input for the SPI interface.<br><b>Hardware Configuration 3.</b> Hardware Control Mode configuration connection.                                 |
| I2C_SDA/SPI_SDI/CONFIG4  | 14    | VDD          | I/O | <b>I2C Control-Port Data.</b> Data input/output for the I2C interface.<br><b>SPI Control-Port Serial Data In.</b> SPI data input.<br><b>Hardware Configuration 4.</b> Hardware Control Mode configuration connection.                                      |
| VDD_OTP                  | 15    | —            | —   | <b>OTP Programming Supply (Input).</b> If VDD = 1.8 V, an external programming supply is required when writing to the OTP memory. This supply can be generated internally if VDD = 3.3 V.  |
| VLDO_OTP/CONFIG6         | 16    | VDD          | I/O | <b>OTP Programming Supply (Output).</b> OTP programming regulator output (VDD = 3.3 V).<br><b>Hardware Configuration 6.</b> Hardware Control Mode configuration connection.  |

### 1.3 Electrostatic Discharge (ESD) Protection Circuitry

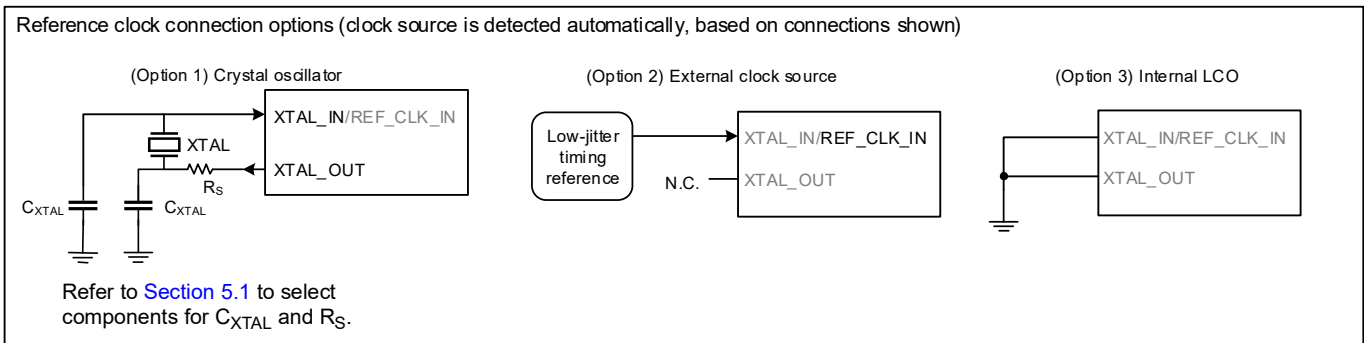
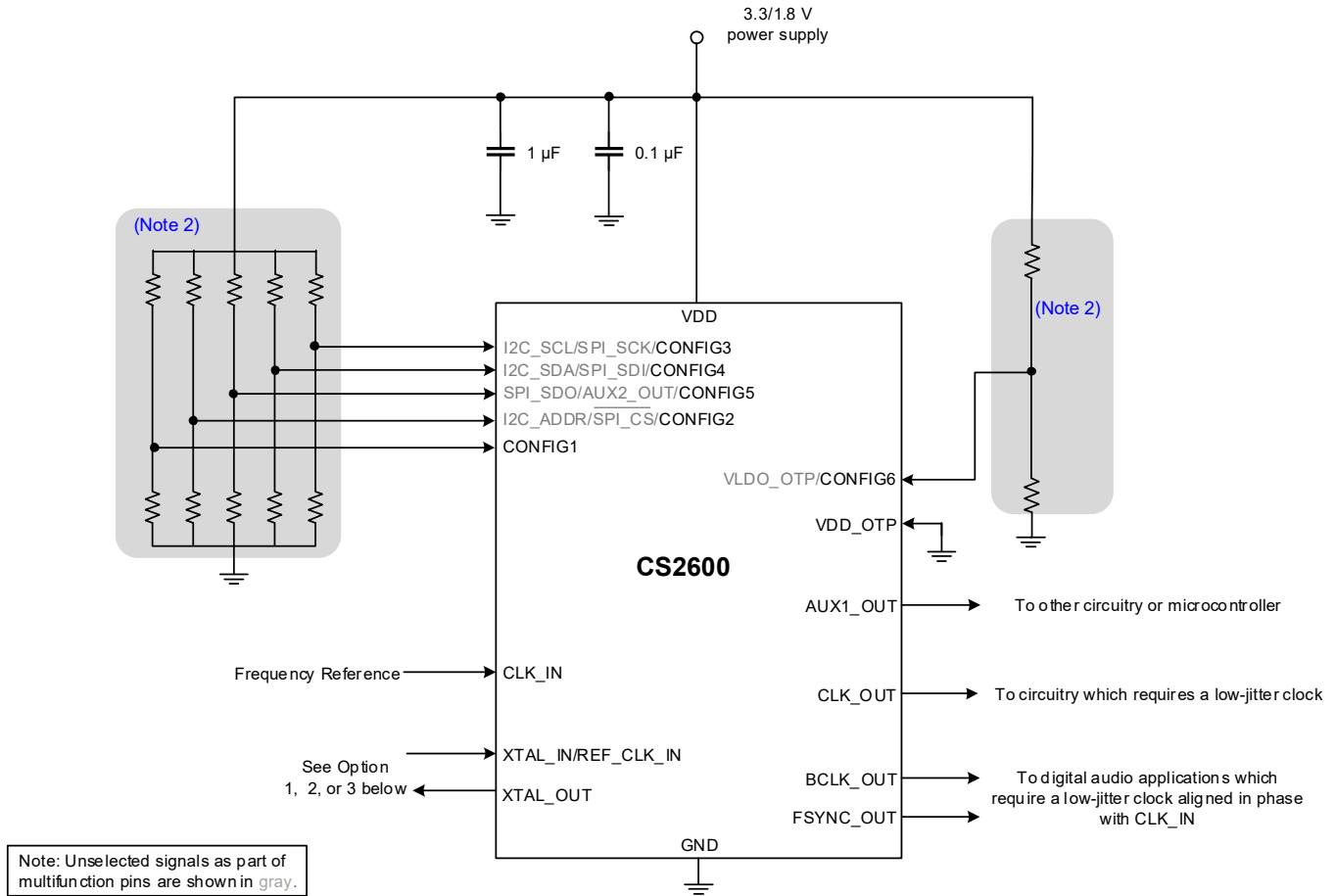


ESD-sensitive device. The CS2600 is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD standards.

## 2 Typical Connections



**Figure 2-1. Typical Connection Diagram—Software Control Mode**



**Figure 2-2. Typical Connection Diagram—Hardware Control Mode**

Notes referenced in the typical connection diagrams:

1. The pull-up resistors are required only for I<sup>2</sup>C operation. The diagram shows 4.7 kΩ pull-up, but higher impedance can be supported depending on clock speed and bus capacitance.
2. Each hardware pin is configured using a pull-up to VDD or pull-down to GND, supporting up to eight configuration options per pin. See Section 4.9 for further detail.

## 3 Characteristics and Specifications

**Table 3-1. Recommended Operating Conditions**

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

| Parameters                            | Symbol              | Min              | Typ  | Max | Units |    |
|---------------------------------------|---------------------|------------------|------|-----|-------|----|
| DC power supply                       | VDD                 | Nominal 3.3 V    | 3.1  | 3.3 | 3.5   | V  |
|                                       |                     | Nominal 1.8 V    | 1.71 | 1.8 | 1.89  | V  |
| OTP programming supply <sup>1,2</sup> | VDD_OTP             | 2.45             | —    | 2.7 | V     |    |
| Supply ramp up/down (all supplies)    | t <sub>PWR_UD</sub> | 0.01             | —    | 10  | ms    |    |
| Ambient temperature                   | T <sub>A</sub>      | Commercial Grade | −40  | —   | 85    | °C |
|                                       |                     | AEC-Q100 Grade 2 | −40  | —   | 105   | °C |

1. The OTP programming supply can be generated by an internal LDO, or else powered externally. To use the internal LDO, the VDD\_OTP pin must be connected to VLDO\_OTP. If VDD < 3.1 V, the OTP programming supply must be powered externally. If OTP programming is not required, VDD\_OTP should be connected to GND.

2. VDD must be present before enabling the VDD\_OTP supply. VDD\_OTP supply must be removed before powering down VDD.

**Table 3-2. Absolute Maximum Ratings**

Test Conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

| Parameters                                       | Symbol            | Min  | Max       | Units |
|--|-------------------|------|-----------|-------|
| DC power supply                                  | VDD               | −0.3 | 4.32      | V     |
| OTP programming supply                           | VDD_OTP           | −0.3 | 2.75      | V     |
| External voltage applied to digital input/output | V <sub>INDI</sub> | −0.3 | VDD + 0.3 | V     |
| Input current                                    | I <sub>in</sub>   | —    | ±10       | mA    |
| Ambient temperature                              | T <sub>A</sub>    | −55  | 125       | °C    |
| Storage temperature                              | T <sub>STG</sub>  | −65  | 150       | °C    |

**Table 3-3. DC Electrical Characteristics**

Test Conditions (unless specified otherwise): T<sub>A</sub> = 25°C; timing reference = 12 MHz (external clock or crystal).

| Parameters                                 | Symbol               | Min         | Typ  | Max        | Units |   |
|--|----------------------|-------------|------|------------|-------|---|
| Power supply current—unloaded <sup>1</sup> | I <sub>VDD</sub>     | —           | 4    | —          | mA    |   |
| OTP programming supply current             | I <sub>VDD_OTP</sub> | —           | —    | 25         | mA    |   |
| Input leakage current (per pin)            | I <sub>IN</sub>      | —           | —    | ±10        | µA    |   |
| Input capacitance (per pin)                | I <sub>C</sub>       | —           | —    | 5          | pF    |   |
| High-level input voltage                   | V <sub>IH</sub>      | 0.70 × VDD  | —    | —          | V     |   |
| Low-level input voltage                    | V <sub>IL</sub>      | —           | —    | 0.30 × VDD | V     |   |
| High-level output voltage                  | V <sub>OH</sub>      | 0.90 × VDD  | —    | —          | V     |   |
| Low-level output voltage                   | V <sub>OL</sub>      | —           | —    | 0.10 × VDD | V     |   |
| VDD power-on reset (POR) threshold         | V <sub>POR</sub>     | VDD rising  | 1.53 | —          | 1.59  | V |
|  |                      | VDD falling | 1.42 | —          | 1.49  | V |
| VDD power-on reset duration <sup>2</sup>   | t <sub>POR</sub>     | 100         | —    | —          | ms    |   |

1. To calculate the additional current consumption due to loading (per output pin), multiply clock output frequency by load capacitance (C<sub>L</sub>) and power supply voltage (VDD).

2. To trigger a power-on reset, VDD must be held below the reset threshold for longer than this duration. Note that VDD interruption shorter than this duration may result in incorrect device behavior.



**Table 3-4. AC Electrical Characteristics**

Test Conditions (unless specified otherwise):  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (commercial grade);  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  (AEC-Q100 grade-2); Load capacitance ( $C_L$ ) = 15 pF.

| Parameters   | Symbol             | Min                                 | Typ       | Max                 | Units                 |                   |
|--|--------------------|-------------------------------------|-----------|---------------------|-----------------------|-------------------|
| Crystal frequency  | $f_{XTAL}$         | REF_CLK_IN_DIV = 10                 | 8         | —                   | 18.75                 | MHz               |
|  |                    | REF_CLK_IN_DIV = 01                 | 16        | —                   | 37.50                 | MHz               |
|  |                    | REF_CLK_IN_DIV = 00                 | 32        | —                   | 50                    | MHz               |
| Crystal interface transconductance ( $T_A = 25^\circ\text{C}$ )  | —                  | VDD = 3.3 V                         | —         | 26                  | —                     | mS                |
|  |                    | VDD = 1.8 V                         | —         | 43                  | —                     | mS                |
| Reference clock input frequency                                  | $f_{REF\_CLK\_IN}$ | REF_CLK_IN_DIV = 10                 | 8         | —                   | 18.75                 | MHz               |
|  |                    | REF_CLK_IN_DIV = 01                 | 16        | —                   | 37.50                 | MHz               |
|  |                    | REF_CLK_IN_DIV = 00                 | 32        | —                   | 75                    | MHz               |
| Reference clock input duty cycle                                 | $D_{REF\_CLK\_IN}$ | 45                                  | —         | 55                  | %                     |                   |
| Clock input frequency  | $f_{CLK\_IN}$      | 50                                  | —         | $30 \times 10^6$    | Hz                    |                   |
| Clock input pulse width  | $PW_{CLK\_IN}$     | $f_{CLK\_IN} < f_{SYSCLK} / 96$ [1] | 2         | —                   | —                     | UI <sup>2</sup>   |
|  |                    | $f_{CLK\_IN} > f_{SYSCLK} / 96$ [1] | 10        | —                   | —                     | ns                |
| CLK_OUT frequency range  | $f_{CLK\_OUT}$     | 6                                   | —         | 75                  | MHz                   |                   |
| BCLK frequency range   | $f_{BCLK\_OUT}$    | $f_{CLK\_OUT} / 48$                 | —         | $f_{CLK\_OUT}$      | MHz                   |                   |
| FSYNC frequency range  | $f_{FSYNC\_OUT}$   | $f_{CLK\_OUT} / 1536$               | —         | $f_{CLK\_OUT} / 16$ | MHz                   |                   |
| Clock output duty cycle  | $t_{OD}$           | 45                                  | 50        | 55                  | %                     |                   |
| Clock output rise time   | $t_{OR}$           | —                                   | 2.5       | —                   | ns                    |                   |
| Clock output fall time   | $t_{OF}$           | —                                   | 2.5       | —                   | ns                    |                   |
| CLK_OUT period jitter <sup>3,4</sup>                             | $t_{JIT}$          | external timing reference           | —         | 40                  | TBD                   | ps <sub>RMS</sub> |
|  |                    | internal oscillator reference       | —         | 35                  | TBD                   | ps <sub>RMS</sub> |
| CLK_OUT baseband TIE jitter <sup>3,5</sup>                       | —                  | external timing reference           | —         | 50                  | TBD                   | ps <sub>RMS</sub> |
|  |                    | internal oscillator reference       | —         | 300                 | TBD                   | ps <sub>RMS</sub> |
| CLK_OUT wideband TIE jitter <sup>3,6</sup>                       | —                  | external timing reference           | —         | 165                 | TBD                   | ps <sub>RMS</sub> |
|  |                    | internal oscillator reference       | —         | 300                 | TBD                   | ps <sub>RMS</sub> |
| PLL lock time—Multiplier Mode                                    | $t_{LC}$           | $f_{CLK\_IN} < 200$ kHz             | —         | 100                 | 200                   | UI <sup>7</sup>   |
|  |                    | $f_{CLK\_IN} > 200$ kHz             | —         | 1                   | 3                     | ms                |
| PLL lock time—Synthesizer Mode                                   | $t_{LR}$           | —                                   | 1         | 3                   | ms                    |                   |
| CLK_OUT frequency resolution <sup>3,8</sup>                      | —                  | high resolution                     | —         | 1                   | —                     | ppm               |
|  |                    | high multiplication                 | —         | 244                 | —                     | ppm               |
| Oscillator frequency   | —                  | 11.76                               | 12.0      | 12.24               | MHz                   |                   |
| Oscillator frequency thermal sensitivity                         | —                  | —                                   | 50        | —                   | ppm/ $^\circ\text{C}$ |                   |
| Oscillator frequency stability (relative to $25^\circ\text{C}$ ) | —                  | $-40$ to $85^\circ\text{C}$         | —0.7      | —                   | 0.7                   | %                 |
|  |                    | $-40$ to $105^\circ\text{C}$        | —0.9      | —                   | 0.7                   | %                 |
| Phase alignment error  | —                  | —                                   | $\pm 0.5$ | —                   | UI <sup>9</sup>       |                   |
| Clock output skew  | —                  | —                                   | —         | $\pm 0.5$           | ns                    |                   |
| Clock output frequency deviation                                 | —                  | —                                   | —         | 0.1                 | %                     |                   |
| Start-up time <sup>10</sup>                                      | —                  | —                                   | —         | 20                  | ms                    |                   |

1. The internal timing reference clock (SYSCLK) is derived from REF\_CLK\_IN (see Section 4.2).

2. UI (unit interval) corresponds to  $t_{SYSCLK}$  or  $1 / f_{SYSCLK}$ .

3. REF\_CLK\_IN is a 12 MHz timing reference clock, with phase noise 20 dB lower than the output clock noise. The clock output frequency ( $f_{CLK\_OUT}$ ) is 24.576 MHz.

4. Sample size is 10000.

5. Using 3rd order 100 Hz–40 kHz bandpass filter as defined in AES-12id-2020 Section 3.4.2.

6. Using 3rd order 100 Hz high pass filter as defined in AES-12id-2020 Section 3.4.1.

7. UI (unit interval) corresponds to  $t_{CLK\_IN}$  or  $1 / f_{CLK\_IN}$ .

8. The frequency accuracy of the PLL clock output is directly proportional to the accuracy of the clock input.

9. UI (unit interval) corresponds to  $t_{CLK\_OUT}$  or  $1 / f_{CLK\_OUT}$ .

10. The time to first locked clock output, assuming OTP configuration for  $f_{CLK\_IN} = 48$  kHz.

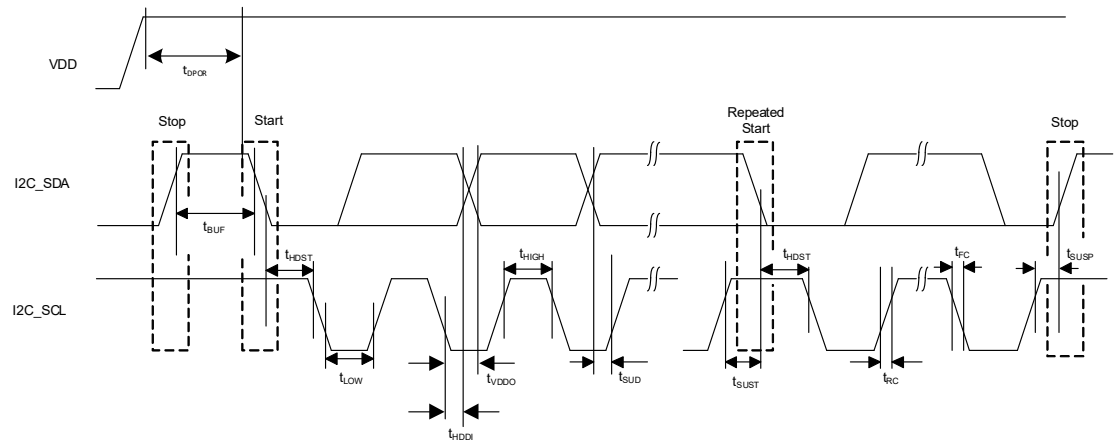
**Table 3-5. Switching Specifications—I2C Control Port**

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at  $V_{IL}$  and  $V_{IH}$  thresholds, output timings are measured at  $V_{OL}$  and  $V_{OH}$  thresholds;  $T_A = 25^\circ\text{C}$ .

| Parameters <sup>1,2</sup>   | Symbol     | Min                               | Max  | Units    |    |
|---|------------|-----------------------------------|------|----------|----|
| SCL clock frequency   | $f_{SCL}$  | —                                 | 1000 | kHz      |    |
| Clock low time  | $t_{LOW}$  | 500                               | —    | ns       |    |
| Clock high time   | $t_{HIGH}$ | 260                               | —    | ns       |    |
| Start condition hold time (before first pulse clock)                          | $t_{HDST}$ | 260                               | —    | ns       |    |
| Setup time for repeated start   | $t_{SUST}$ | 260                               | —    | ns       |    |
| Rise time of SCL and SDA  | $t_{RC}$   | $f_{SCL} \leq 100$ kHz            | 600  | 1000     | ns |
|   |            | 100 kHz < $f_{SCL} \leq 400$ kHz  | 180  | 300      | ns |
|   |            | 400 kHz < $f_{SCL} \leq 1000$ kHz | 72   | 120      | ns |
| Fall time SCL and SDA   | $t_{FC}$   | $f_{SCL} \leq 100$ kHz            | 6.5  | 300      | ns |
|   |            | 100 kHz < $f_{SCL} \leq 400$ kHz  | 6.5  | 300      | ns |
|   |            | 400 kHz < $f_{SCL} \leq 1000$ kHz | 6.5  | 120      | ns |
| Rise time variation between SDA and SCL                                       | —          | —                                 | 1.67 | x        |    |
| Fall time variation between SDA and SCL                                       | —          | $f_{SCL} \leq 100$ kHz            | —    | 100      | ns |
|   |            | 100 kHz < $f_{SCL} \leq 400$ kHz  | —    | 100      | ns |
|   |            | 400 kHz < $f_{SCL} \leq 1000$ kHz | —    | 75       | ns |
| Setup time for stop condition   | $t_{SUSP}$ | 260                               | —    | ns       |    |
| SDA setup time to SCL rising  | $t_{SUD}$  | 50                                | —    | ns       |    |
| SDA input hold time from SCL falling  | $t_{HDDI}$ | 0                                 | —    | ns       |    |
| Output data valid (Data/ACK)  | $t_{VDDO}$ | $f_{SCL} \leq 100$ kHz            | —    | 3450     | ns |
|   |            | 100 kHz < $f_{SCL} \leq 400$ kHz  | —    | 900      | ns |
|   |            | 400 kHz < $f_{SCL} \leq 1000$ kHz | —    | 450      | ns |
| Bus free time between transmissions   | $t_{BUF}$  | 500                               | —    | ns       |    |
| SDA bus capacitance   | $C_B$      | —                                 | 400  | pF       |    |
| SCL/SDA pull-up resistance  | $R_P$      | 500                               | —    | $\Omega$ |    |
| Pulse width of spikes to be suppressed  | $t_{ps}$   | 0                                 | 50   | ns       |    |
| Start-up time from power-up/software reset to control port ready <sup>3</sup> | $t_{DPOR}$ | —                                 | 5    | ms       |    |

1. The I2C control port uses a 16-bit register address and 16-bit data words.

2. I2C control-port timing.



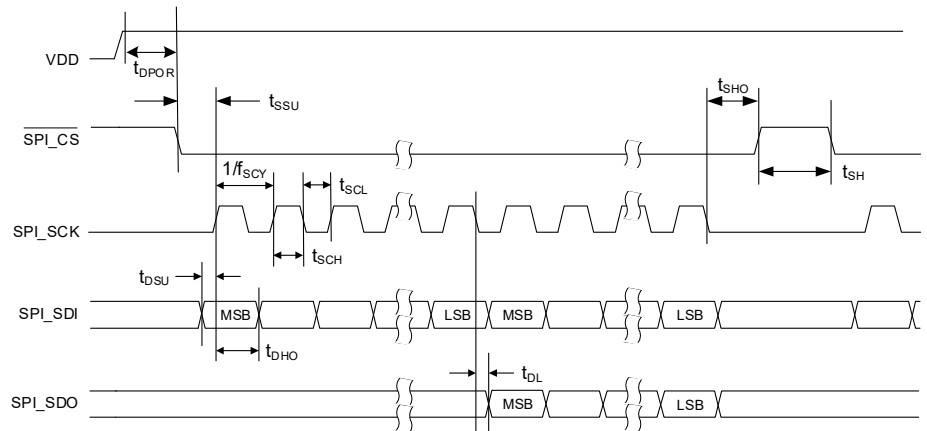
3. Time from power-up measured from when VDD is within the recommended operating conditions (see Table 3-1).

**Table 3-6. Switching Specifications—SPI Control Port**

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at  $V_{IL}$  and  $V_{IH}$  thresholds, output timings are measured at  $V_{OL}$  and  $V_{OH}$  thresholds;  $T_A = 25^\circ\text{C}$ .

| Parameters <sup>1,2</sup>   | Symbol     | Min  | Max  | Units |
|---|------------|------|------|-------|
| SCK clock frequency   | $f_{SCL}$  | —    | 4.5  | MHz   |
| Access to OTP registers (0x2300–0x232F)                             |            | —    | 17.5 | MHz   |
| Access to all other registers                                       |            |      |      |       |
| CS falling edge to SCK rising edge                                  | $t_{SSU}$  | 5    | —    | ns    |
| SCK falling edge to CS rising edge                                  | $t_{SHO}$  | 0.5  | —    | ns    |
| SCK pulse width low   | $t_{SCL}$  | 18.5 | —    | ns    |
| SCK pulse width high  | $t_{SCH}$  | 18.5 | —    | ns    |
| SDI to SCK rising setup time  | $t_{DSU}$  | 5    | —    | ns    |
| SDI to SCK hold time  | $t_{DHO}$  | 2.5  | —    | ns    |
| SCK falling edge to SDO transition                                  | $t_{DL}$   | 0    | 15   | ns    |
| CS rising edge to SDO output high-Z                                 | —          | 0    | 20   | ns    |
| Bus free time between active CS                                     | $t_{SH}$   | 110  | —    | ns    |
| Delay from supply voltage stable to control port ready <sup>3</sup> | $t_{DPOR}$ | —    | 5    | ms    |

1. The SPI control port uses a 15-bit register address and 16-bit data words.
2. SPI control-port timing.



3. The supply voltage is considered stable when VDD is within the recommended operating conditions (see [Table 3-1](#)).

## 4 Functional Description

### 4.1 Device Architecture

The CS2600 is a highly versatile clock generator. It combines an analog PLL and digital FLL to provide high-resolution clock multiplier and clock synthesizer capability. The delta-sigma architecture enables low-jitter clock generation across a wide range of fractional operating ratios; it also supports fast transitions between different ratios and output frequencies. Configurable bandwidth of the digital FLL enables optimized behavior under dynamic operating conditions.

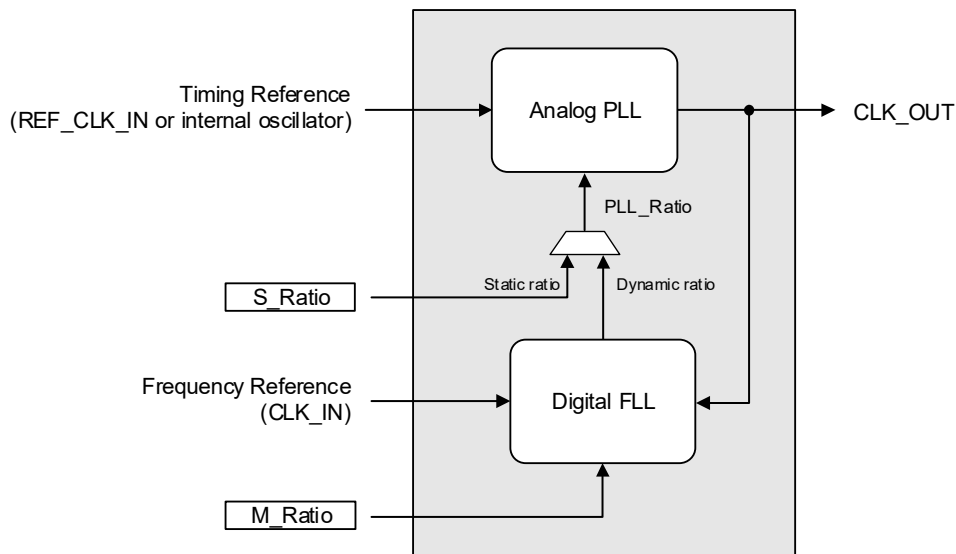
The analog PLL generates the main clock output (CLK\_OUT), using the timing reference as its input. The timing reference is a stable low-jitter clock source, derived from the REF\_CLK\_IN input, external crystal, or the internal oscillator. The timing reference is used to ensure the time and phase stability of the PLL output. The PLL frequency ratio determines the multiplier ratio between the timing-reference input and the clock output.

The digital FLL provides input to the analog PLL to configure the frequency ratio. The digital FLL uses the frequency reference (CLK\_IN) as its input and generates the PLL frequency ratio as a control signal to the analog PLL. The capability of the digital FLL is enhanced by its configurable bandwidth; a wide bandwidth is used to achieve lock in a short time, while a narrow bandwidth is used to provide optimal jitter performance.

The CS2600 can be configured in Multiplier Mode or Synthesizer Mode.

- In Multiplier Mode, the user-selected ratio is an input to the digital FLL and defines the CLK\_OUT:CLK\_IN frequency ratio. The FLL monitors the input and output clocks and controls the analog PLL frequency ratio to achieve the required CLK\_OUT frequency. The frequency ratio is dynamically controlled to maintain the required output ratio.
- In Synthesizer Mode, the user-selected ratio is an input to the analog PLL and defines the CLK\_OUT:REF\_CLK\_IN frequency ratio (or CLK\_OUT:oscillator frequency ratio). The analog PLL frequency ratio is configured directly by the respective control fields. The output clock is generated from the timing reference alone, with no other clock input required. Note that the digital FLL is not used in Synthesizer Mode.

The hybrid analog/digital PLL is illustrated in Fig. 4-1. In Multiplier Mode, the user-defined ratio is defined by the *M\_Ratio* parameter. In Synthesizer Mode, the user-defined ratio is defined by the *S\_Ratio* parameter.



**Figure 4-1. Hybrid Analog/Digital PLL**

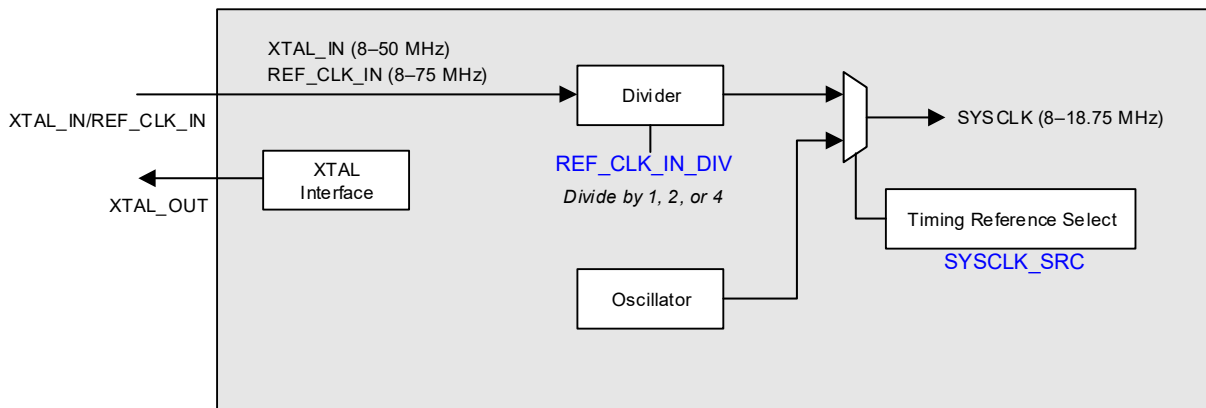
## 4.2 Timing Reference Configuration

The low-jitter timing reference is provided either by an external source (clock input or crystal), or by the internal oscillator. By default, the timing reference is selected automatically depending on the external pin connections, as shown Section 2. It is recommended to use `SYSCLK_SRC` to select the internal or external source, as shown in Fig. 4-2.

The frequency range for the external timing reference is described in Table 3-4. Note that the supported frequency range differs depending on the applicable source.

The internal timing reference, `SYSCLK`, is derived from the selected timing source. A programmable divider is provided for the external timing reference; the divider must be configured using `REF_CLK_IN_DIV` to bring the reference frequency within the valid `SYSCLK` range of 8–18.75 MHz.

The timing reference configuration is shown in Fig. 4-2.



**Figure 4-2. Timing Reference Configuration**

Note that, in Synthesizer Mode, the PLL ratio defines the `CLK_OUT`:`REF_CLK_IN` frequency ratio (or `CLK_OUT`:oscillator frequency ratio, if the oscillator is selected as the timing reference). The timing-reference divider has no effect on this, and does not need to be considered when calculating the desired frequency ratio.

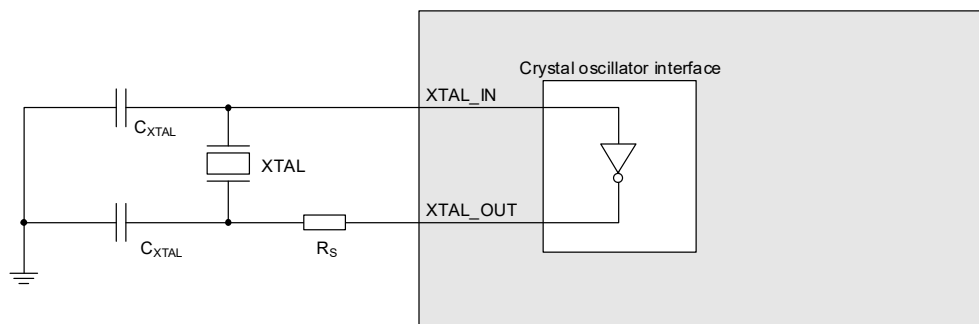
### 4.2.1 REF\_CLK\_IN Detection and Indication

The `REF_CLK_IN` signal is monitored to confirm the timing reference is present.

The `REF_CLK_IN` presence is indicated using `ERR_STS3`. This bit is a latching bit—it is set when `REF_CLK_IN` is not present, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if `REF_CLK_IN` is not present.

### 4.2.2 Crystal Oscillator

The crystal oscillator uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 4-3. A series resistor ( $R_S$ ) may also be required to configure the drive level for the selected crystal.



**Figure 4-3. Crystal Oscillator Connection**

Guidance on selecting a suitable crystal and associated components is provided in [Section 5.1](#). The suitability of the external crystal is calculated as a function of the operating voltage (VDD) and the transconductance of the crystal interface, as defined in [Table 3-4](#).

## 4.3 Hybrid PLL Configuration

The PLL is enabled and configured as described in the following sections.

### 4.3.1 Enable and Lock Status

The PLL is enabled by setting [PLL\\_EN1](#) and [PLL\\_EN2](#) (both bits must be set in order to enable the PLL). Note there are no sequencing requirements—the bits may be set or cleared in any order.

**Note:** The device should be fully configured by writing to the applicable control registers before enabling the PLL. When changing the configuration, it is recommended to disable the PLL before updating the register fields; this ensures there is no unexpected transient behavior. See [Section 4.7.3](#) for further details of configuration restrictions.

The PLL lock status is dependent on the clock inputs and the device configuration. Changes in the clock inputs or to the configuration registers can cause the PLL to lose lock. If the PLL loses lock, the quality of the clock outputs cannot be assured.

The PLL lock status is indicated using [F\\_UNLOCK](#). This bit is set if the PLL is not frequency locked (including if the PLL is disabled). The lock status can be indicated on an auxiliary output pin as described in [Section 4.6](#). The lock status can be used to automatically disable the clock outputs—see [Section 4.5.4](#) for further details.

The PLL lock status is also indicated using [F\\_UNLOCK\\_STICKY](#). This is a latching bit—it is set when [F\\_UNLOCK](#) is set, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if [F\\_UNLOCK](#) is set.

### 4.3.2 Ratio Configuration

The PLL is configured using a ratio that determines the output frequency as a function of either the timing reference, [REF\\_CLK\\_IN](#), (in Synthesizer Mode) or the frequency reference, [CLK\\_IN](#), (in Multiplier Mode).

- In Synthesizer Mode, the output frequency is defined by the following equation:

$$f_{\text{CLK\_OUT}} = f_{\text{REF\_CLK\_IN}} \times \text{PLL Ratio}$$

For example, to generate a 24.576 MHz output from a 12 MHz timing reference, a ratio of 2.048 is required.

- In Multiplier Mode, the output frequency is defined by the following equation:

$$f_{\text{CLK\_OUT}} = f_{\text{CLK\_IN}} \times \text{PLL Ratio}$$

For example, to generate a 24.576 MHz output from a 48 kHz frequency reference, a ratio of 512 is required.

The PLL ratio is a 32-bit value, configured using the [RATIO<sub>n</sub>](#) fields. A maximum of four different ratios can be configured, allowing the device to switch easily between different use cases. The applicable ratio is selected using [S\\_RATIO\\_SEL](#) (in Synthesizer Mode) or [M\\_RATIO\\_SEL](#) (in Multiplier Mode).

In Multiplier Mode, the PLL ratio can be defined in high-resolution (12.20) or high-multiplication (20.12) format; the format is selected using [RATIO\\_CFG](#). In Synthesizer Mode, the high-resolution (12.20) format is used.

- In high-resolution (12.20) format, the 12 MSBs represent the integer portion of the ratio, and the remaining 20 bits represent the fractional portion. This format supports a maximum multiplication factor of ~4096, with a resolution of 0.954 ppm.
- In high-multiplication (20.12) format, the 20 MSBs represent the integer portion of the ratio, and the remaining 12 bits represent the fractional portion. This format supports a maximum multiplication factor of ~1,048,576, with a resolution of 244 ppm.

**Note:** If the desired ratio is less than 4096, the 12.20 format is recommended, to ensure the accuracy of the PLL output.

The PLL ratio is also configured using [RATIO\\_MOD](#), allowing additional multiplication/division factors to be applied to the [RATIO<sub>n</sub>](#) selection.

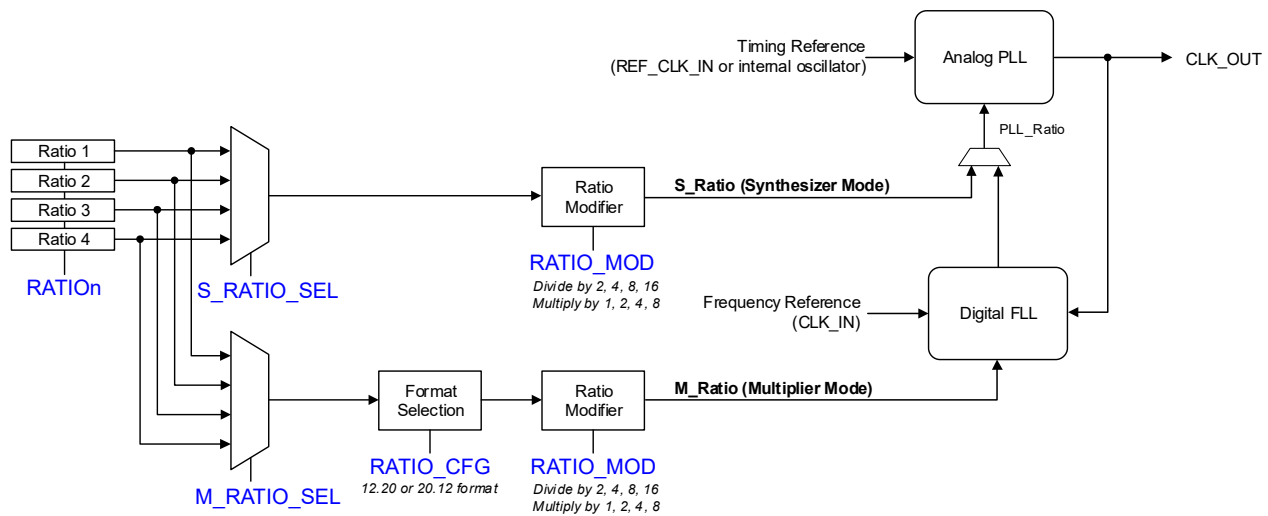
The ratio modifier can be used to simplify the selection of related frequency ratios, while using the same **RATIO<sub>n</sub>** value. It can also be used to support high multiplication ratios in 12.20 format (multiplying by 2, 4, or 8) or to enable greater precision in 20.12 format (dividing by 2, 4, 8, or 16).

Note that, regardless of the ratio format and the ratio modifier, the PLL ratio cannot exceed a multiplication factor of 1,048, 576 or a resolution of 0.954 PPM. If the configured parameters exceed these limits, the effective multiplication or resolution is truncated.

If the selected PLL ratio is invalid, the output clocks are disabled. Normal operation resumes when a valid ratio is detected (either due to register configuration or a change in **CLK\_IN** frequency).

An invalid ratio is indicated using **ERR\_STS6**. This bit is a latching bit—it is set when an invalid configuration is detected and remains set until a 1 is written to the bit. Note the bit cannot be cleared if the configuration is invalid.

The ratio configuration is illustrated in Fig. 4-4.



**Figure 4-4. PLL Ratio Configuration**

**Notes:** In Synthesizer Mode, the selected **S\_Ratio** defines the **CLK\_OUT:REF\_CLK\_IN** frequency ratio (or **CLK\_OUT:oscillator** frequency ratio, if the oscillator is selected as the timing reference). The timing-reference divider (see Section 4.2) has no effect on this, and does not need to be considered when calculating the desired frequency ratio.

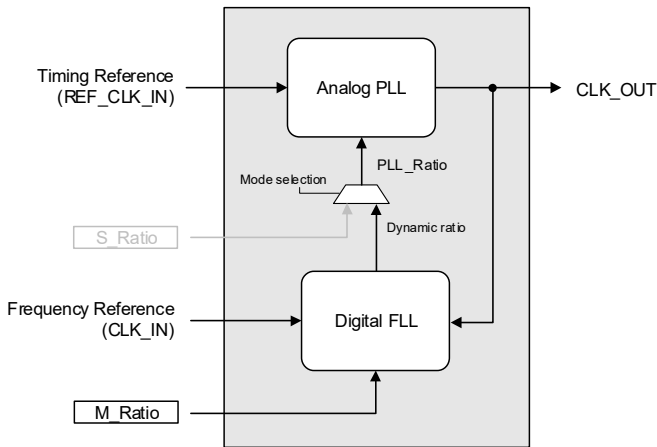
In Multiplier Mode, if automatic rate control (ARC) is enabled, the frequency ratio is configured automatically depending on the selected **CLK\_OUT** frequency and the detected **CLK\_IN** frequency. The **RATIO<sub>n</sub>** and **RATIO\_MOD** fields are not used if ARC is enabled. See Section 4.4.4 for details of the ARC function.

### 4.3.3 Mode Selection

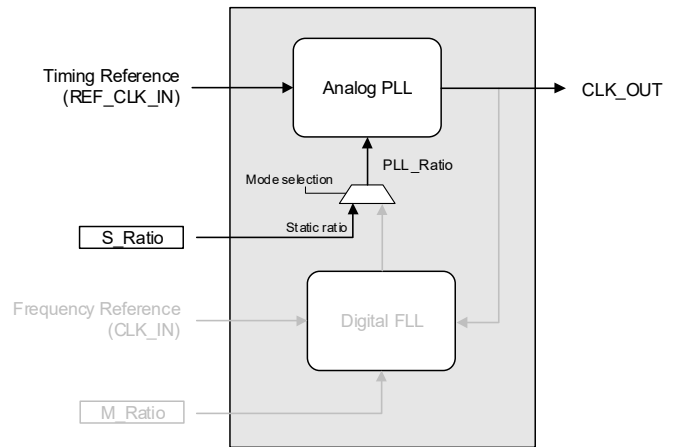
The hybrid PLL architecture supports Multiplier Mode and Synthesizer Mode functions. The CS2600 can also be configured in Smart Multiplier Mode, with the ability to switch automatically between modes.

- In Multiplier Mode, the **CLK\_IN** signal provides the frequency reference. The user-selected ratio defines the **CLK\_OUT:CLK\_IN** frequency ratio. The PLL is dynamically controlled to maintain the required output ratio.
- In Synthesizer Mode, the **REF\_CLK\_IN** signal provides the input reference. The user-selected ratio defines the **CLK\_OUT:REF\_CLK\_IN** frequency ratio. The PLL is controlled using a static ratio derived from the respective control fields.
- In Smart Multiplier Mode, the CS2600 selects Multiplier Mode or Synthesizer Mode depending on the status of the **CLK\_IN** frequency reference. The adaptive behavior can be used to accommodate periods where the frequency reference is unstable or not present.

The hybrid-PLL operating modes are illustrated in Fig. 4-5 and Fig. 4-6.



**Figure 4-5. Multiplier Mode**



**Figure 4-6. Synthesizer Mode**

To select Synthesizer Mode or Multiplier Mode, the `S_RATIO_SEL` and `M_RATIO_SEL` fields must both be set to the same value. Under this condition, the operating mode is selected using `PLL_MODE_SEL`.

Smart Multiplier Mode is selected if `S_RATIO_SEL` and `M_RATIO_SEL` are set to different values. Under this condition, the operating mode is configured automatically.

In Smart Multiplier Mode, the device normally operates in Multiplier Mode. Synthesizer Mode may be used during PLL start-up, if `CLK_IN` is not present; the behavior is selectable using the ratio configuration fields.

- If the ratio selected by `S_RATIO_SEL` is zero, Synthesizer Mode is not valid. In this case, the clock output starts when a valid reference is present at `CLK_IN`; there is no clock output until `CLK_IN` is present. When `CLK_IN` is present, Multiplier Mode is enabled and is used thereafter, including if `CLK_IN` is subsequently interrupted.
- If the ratio selected by `S_RATIO_SEL` is nonzero, Synthesizer Mode is selected during PLL start-up, if `CLK_IN` is not present. When `CLK_IN` is present, the CS2600 makes a glitchless transition to Multiplier Mode and remains in this mode thereafter, including if `CLK_IN` is subsequently interrupted.

See Section 4.4 for further details of the CS2600 behavior when the `CLK_IN` input is missing or unstable.

## 4.4 Frequency Reference Configuration

The frequency reference (`CLK_IN`) is an input to the digital FLL, which is used to generate the dynamic ratio for the analog PLL. The digital FLL monitors the input and output clocks and controls the analog PLL frequency ratio to achieve the required `CLK_OUT` frequency. The hybrid PLL/FLL architecture allows the low-jitter timing reference to be used to generate the clock output, while using a separate clock (`CLK_IN`) as a frequency reference. The frequency range for `CLK_IN` is defined in Table 3-4.

The CS2600 is tolerant of intermittent or unstable characteristics on the `CLK_IN` frequency reference. The behavior of the device is configurable as described in the following sections.

### 4.4.1 `CLK_IN` Detection and Indication

The `CLK_IN` signal is monitored to confirm the frequency reference is present and stable.

The `CLK_IN` presence is indicated using `ERR_STS1`. This bit is a latching bit—it is set when `CLK_IN` is not present, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if `CLK_IN` is not present.

The `CLK_IN` stability is indicated using `ERR_STS2`. This bit is a latching bit—it is set when `CLK_IN` is unstable or not present, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if `CLK_IN` is unstable or not present.

The `CLK_IN` status can be indicated on an auxiliary output pin as described in Section 4.6.



### 4.4.2 Holdover Mode

The CLK\_IN signal is monitored to confirm the frequency reference is present and stable. The holdover function enables a valid clock output to be maintained under conditions where the reference is missing or unstable. The holdover function is enabled automatically in Smart Multiplier Mode. See [Section 4.3.3](#) to select Smart Multiplier Mode.

**Notes:** If Smart Multiplier Mode is selected, Synthesizer Mode may be used during PLL start-up, if CLK\_IN is not present. The holdover function is not supported until a valid CLK\_IN has been detected and the CS2600 automatically transitions to Multiplier Mode.

In Multiplier Mode (Smart Multiplier Mode not selected), the PLL remains unlocked indefinitely while CLK\_IN is interrupted. When CLK\_IN resumes, the PLL locks to CLK\_IN and the valid CLK\_OUT signal is restored.

If CLK\_IN is missing or unstable, the CS2600 freezes the dynamic PLL ratio at its current setting. The PLL remains locked and the CLK\_OUT signal continues without any glitch or interruption.

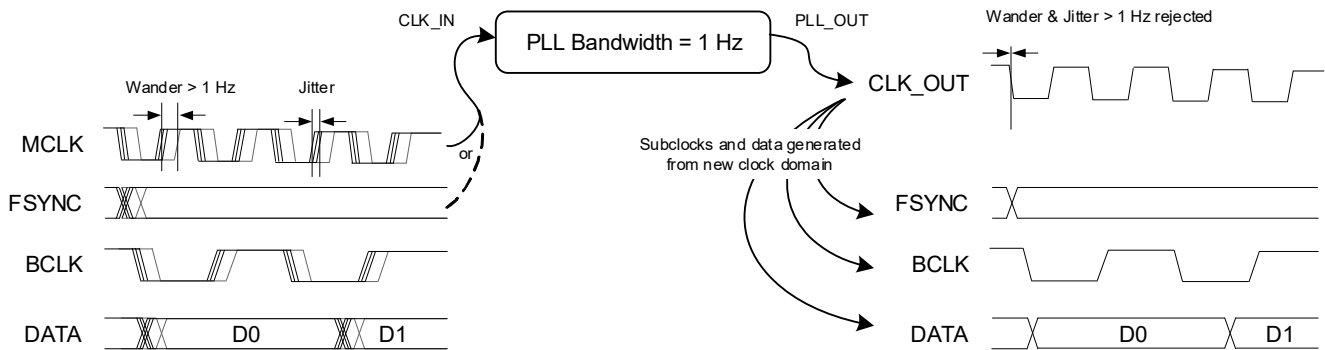
When a valid CLK\_IN is detected, the PLL resynchronizes to the frequency reference. If the frequency reference aligns with the previous CLK\_IN frequency, the PLL remains locked and maintains a glitchless output.

### 4.4.3 Digital FLL Bandwidth

The bandwidth of the digital FLL can be configured to suit different operating conditions. The FLL bandwidth determines the extent to which any jitter on the CLK\_IN signal is attenuated or is passed through to the output clocks. In some applications, it is desirable to reject all jitter as far as possible; in other applications, it may be preferable to preserve the low-frequency variations in the reference clock while attenuating jitter at higher frequencies.

The loop bandwidth is configured using [FLL\\_BW](#) and [FLL\\_BW\\_MOD](#). The [FLL\\_BW](#) field selects a value 1–128 Hz; the [FLL\\_BW\\_MOD](#) selects multiplication factor of  $\times 1$  or  $\times 16$ . The combination of two fields allows bandwidth selections in the range 1–2048 Hz.

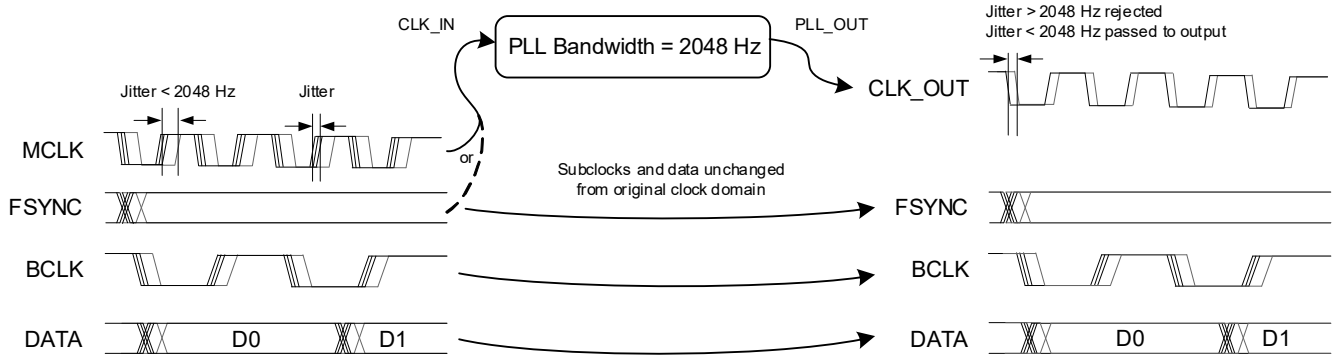
A narrow bandwidth is typically recommended in applications where the CLK\_OUT signal provides a new clock domain from which all other system clocks are derived. In these circumstances, the system benefits from maximum jitter rejection, as illustrated in [Fig. 4-7](#).



**Figure 4-7. Narrow Bandwidth Application**

A wide bandwidth is typically recommended in applications where some of the system clocks are referenced to CLK\_OUT, while others are derived from CLK\_IN. In these circumstances, it may be necessary to preserve some of the input reference variation in the clock output, in order to maintain phase alignment.

The FLL bandwidth should be set to the lowest setting that does not cause system-timing errors between the CLK\_IN and CLK\_OUT domains. The wide bandwidth use case is illustrated in Fig. 4-8.



**Figure 4-8. Wide Bandwidth Application**

#### 4.4.4 Automatic Rate Control (ARC)

The CS2600 supports an automatic rate control (ARC) function which detects the CLK\_IN reference frequency and configures the PLL multiplier ratio for the required PLL output frequency. Auto-detection is supported across a range of sample-rate frequencies typically used in digital audio systems.

The ARC supports seamless transitions through changes in the reference frequency. The BCLK and FSYNC outputs (see Section 4.5.2) are controlled automatically to accommodate changes in CLK\_IN frequency.

**Note:** Automatic rate control is supported in Multiplier Mode only (see Section 4.3.3). If Synthesizer Mode is selected, ARC should be disabled at all times. If Smart Multiplier Mode is selected, and the ratio selected by S\_RATIO\_SEL is nonzero, ARC should be disabled at all times.

Automatic rate control is enabled using ARC\_EN. If ARC is enabled, the CS2600 automatically detects the CLK\_IN reference as one of the valid input frequencies. The PLL output frequency is configured using ARC\_MCLK; the PLL output (MCLK) frequency follows the same base frequency as the input reference, as described in Table 4-1.

**Table 4-1. ARC Configuration**

| CLK_IN Frequency                      | ARC_MCLK | PLL Output Frequency |
|---------------------------------------|----------|----------------------|
| 32 kHz, 48 kHz,<br>96 kHz, or 192 kHz | 00       | 12.288 MHz           |
|                                       | 01       | 24.576 MHz           |
|                                       | 10       | 49.152 MHz           |
|                                       | 11       | —                    |
| 44.1 kHz, 88.2 kHz,<br>or 176.4 kHz   | 00       | 11.2896 MHz          |
|                                       | 01       | 22.5792 MHz          |
|                                       | 10       | 45.1584 MHz          |
|                                       | 11       | —                    |

The ARC automatically adjusts for changing CLK\_IN reference frequencies. The input reference can be stopped and then restarted at the new frequency, or the input reference can change frequency without interruption.

Detection of a new CLK\_IN frequency takes a maximum of 24 stable CLK\_IN periods. The PLL remains locked provided the CLK\_IN frequency transition is an exact integer ratio (increasing or decreasing). The PLL output is stable to within 0.1% during these transitions. In the case of 32–48 kHz transitions, an exact 1.5 ratio transition is also supported without losing PLL lock. For example, the PLL remains locked for 48.2–96.4 kHz transitions, or 48.3–32.2 kHz transitions; seamless operation is not assured for 48.2–96.0 kHz transitions, or 48.0–44.1 kHz transitions.

Note that, if the CLK\_IN reference changes frequency without interruption, the new frequency must be established within five CLK\_IN periods to ensure stable operation. If the input reference is stopped when changing frequency, the CS2600 must be configured in Smart Multiplier Mode (see Section 4.3.3) to ensure uninterrupted PLL operation.

If ARC is enabled, the FSYNC output is automatically configured to align with the CLK\_IN reference frequency. The duty cycle is configured using [FSYNC\\_DUTY\\_CYCLE](#).

If ARC is enabled, the BCLK output is configured using [ARC\\_BCLK\\_DIV](#). The frequency can be configured as a ratio of the PLL output (MCLK) or else as a multiple of the FSYNC rate.

**Note:** BCLK output is only supported for valid divisions of the MCLK frequency (valid divisions of the MCLK frequency are defined by the [BCLK\\_DIV](#) field options). If the ratio calculated by the ARC is not supported, the output clocks are disabled. Normal operation resumes when a valid configuration is detected (due to register write or change in CLK\_IN frequency).

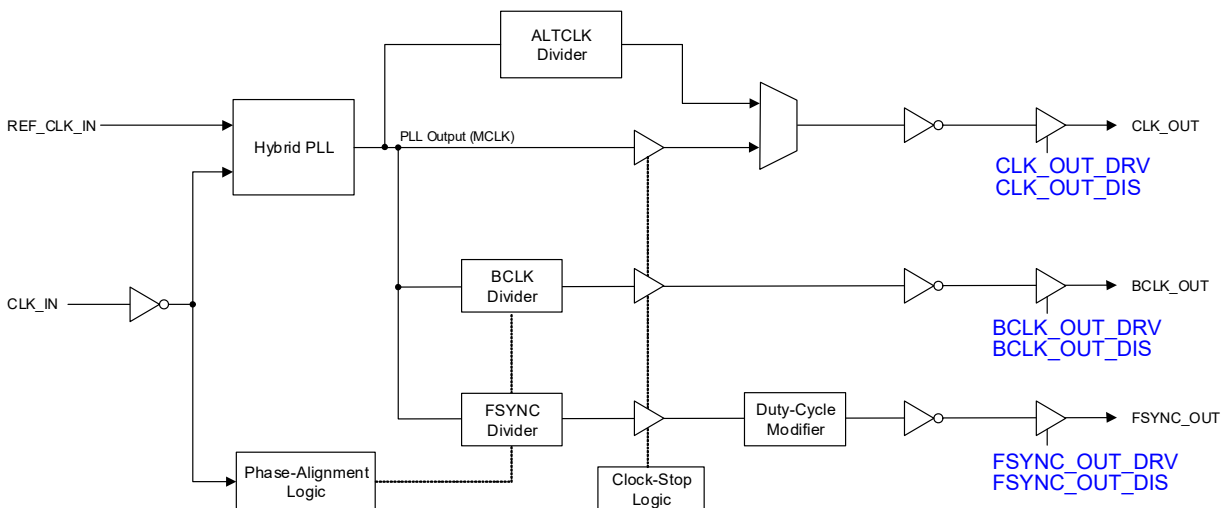
An invalid configuration is indicated using [ERR\\_STS6](#). This bit is a latching bit—it is set when an invalid configuration is detected and remains set until a 1 is written to the bit. Note the bit cannot be cleared if the configuration is invalid.

The CS2600 provides a glitchless transition following a change in CLK\_IN frequency; the FSYNC and BCLK outputs are reconfigured seamlessly at the end of a FSYNC period.

## 4.5 Output Configuration

The CS2600 provides three clock outputs. The main output from the PLL is provided on the CLK\_OUT pin. Two additional clock signals, BCLK\_OUT and FSYNC\_OUT, are derived from the main PLL output and are intended to support digital-audio applications.

The clock outputs are illustrated in [Fig. 4-9](#).



**Figure 4-9. Clock Outputs**

Each clock output can be enabled independently using the respective control field [CLK\\_OUT\\_DIS](#), [BCLK\\_OUT\\_DIS](#), or [FSYNC\\_OUT\\_DIS](#). If an output is disabled, the respective driver is configured in a high-impedance (Hi-Z) state.

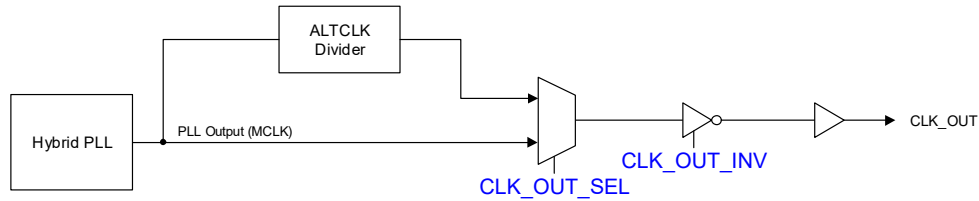
The drive strength for the clock outputs is configurable using the respective control field [CLK\\_OUT\\_DRV](#), [BCLK\\_OUT\\_DRV](#), or [FSYNC\\_OUT\\_DRV](#).

### 4.5.1 CLK\_OUT Configuration

The ALTCLK generator is an automatic divider that can be used to generate a fixed CLK\_OUT frequency from a range of related PLL frequencies.

The CLK\_OUT signal can be derived either directly from the PLL or else from the ALTCLK generator. The clock source is selected using [CLK\\_OUT\\_SEL](#).

The polarity of the CLK\_OUT signal can be inverted using `CLK_OUT_INV`. The inversion applies regardless of the CLK\_OUT source, as shown in [Fig. 4-10](#).



**Figure 4-10. CLK\_OUT Selection**

If ALTCLK is selected as the clock source, the CLK\_OUT frequency is generated as described in [Table 4-2](#). Note that the PLL must be configured for one of the supported frequencies, using the applicable ratio in Multiplier or Synthesizer mode.

**Table 4-2. CLK\_OUT Frequency Select**

| PLL Frequency   | CLK_OUT_SEL | CLK_OUT Frequency |
|---|-------------|-------------------|
| Any   | 00          | = PLL output      |
| 5.6448 MHz, 11.2896 MHz,<br>22.5792 MHz, or 45.1584 MHz | 01          | 352.8 kHz         |
|   | 10          | 1.882 MHz         |
|   | 11          | 2.053 MHz         |
| 6.144 MHz, 12.288 MHz,<br>24.576 MHz, or 49.152 MHz     | 01          | 384 kHz           |
|   | 10          | 2.048 MHz         |
|   | 11          | 2.234 MHz         |

**Notes:**

- If `CLK_OUT_SEL` = 11, the PLL frequencies 5.6448 / 6.144 MHz are not supported
- If `CLK_OUT_SEL` = 11, the PLL frequencies 11.2896 / 12.288 MHz result in 45% output duty cycle

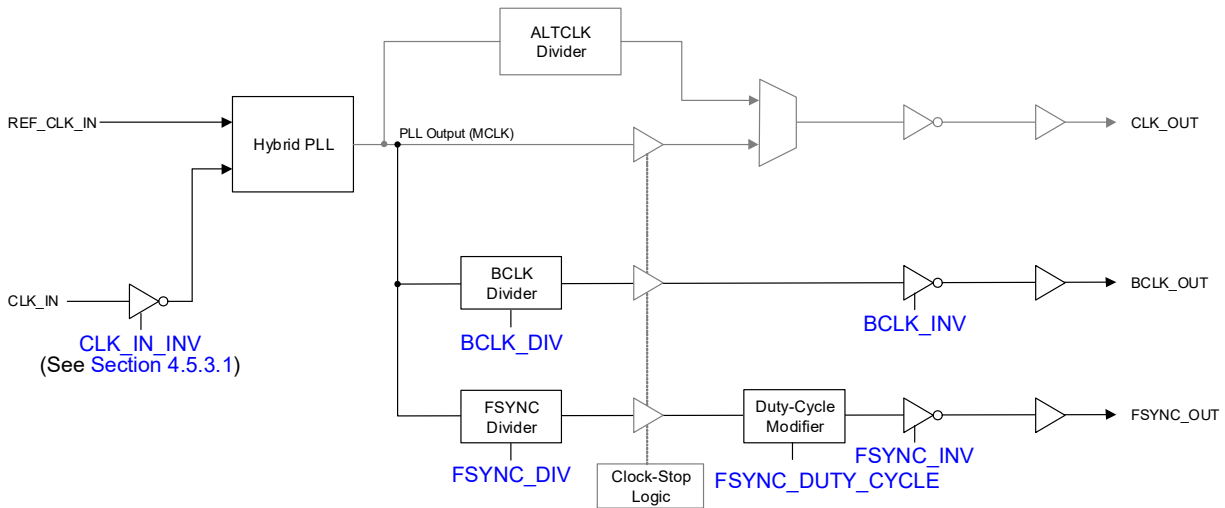
The ALTCLK generator is supported in Synthesizer Mode and Multiplier Mode. If the Holdover function is enabled (see [Section 4.4.2](#)) the PLL output is maintained under conditions where the reference is missing or unstable. Note that the clock-stop logic (see [Section 4.5.4](#)) does not affect the ALTCLK output.

## 4.5.2 BCLK and FSYNC Configuration

The CS2600 supports BCLK and FSYNC outputs, intended for use in digital-audio applications. These clock outputs are derived from the main PLL output (MCLK) using configurable dividers.

**Note:** The BCLK and FSYNC outputs are derived from the PLL output, regardless of whether ALTCLK is selected as the CLK\_OUT source (see [Section 4.5.1](#)).

The BCLK and FSYNC outputs are shown in Fig. 4-11.



**Figure 4-11. BCLK and FSYNC Outputs**

The FSYNC frequency is configured using **FSYNC\_DIV**. The frequency is defined as a ratio of the PLL output (MCLK). The duty cycle is configured using **FSYNC\_DUTY\_CYCLE**.

The BCLK frequency is configured using **BCLK\_DIV**. Note that, for digital-audio applications, the BCLK frequency must be a valid integer multiple of the FSYNC frequency.

**Note:** If automatic rate control (ARC) is enabled, the BCLK frequency is configured using **ARC\_BCLK\_DIV**, and the FSYNC frequency is automatically aligned to the CLK\_IN frequency reference. The **BCLK\_DIV** and **FSYNC\_DIV** fields are not used if ARC is enabled. See Section 4.4.4 for details of the ARC function.

The polarity of the BCLK and FSYNC outputs can be inverted using **BCLK\_INV** and **FSYNC\_INV** respectively. The polarity inversion can be used to support different digital-audio interface formats.

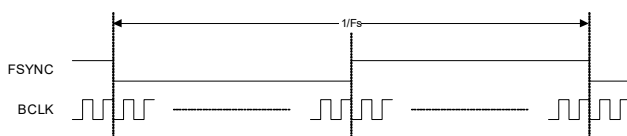
The recommended configuration for different digital-audio formats is defined in Table 4-3.

**Table 4-3. Clock Configuration for Digital Audio Formats**

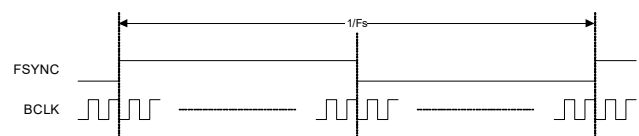
| Digital Audio Format           | BCLK_INV     | FSYNC_INV        | FSYNC_DUTY_CYCLE         |
|--------------------------------|--------------|------------------|--------------------------|
| I2S                            | 1 (inverted) | 1 (inverted)     | 000 (50% duty cycle)     |
| Left-Justified/Right-Justified | 1 (inverted) | 0 (not inverted) | 000 (50% duty cycle)     |
| TDM                            | 1 (inverted) | 0 (not inverted) | As required <sup>1</sup> |

1. Note the FSYNC duty cycle must be configured less than or equal to 50%.

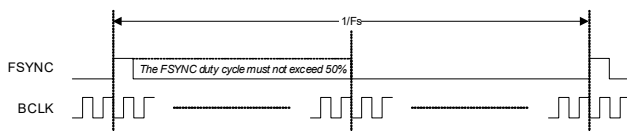
Typical clock signals for different digital-audio formats are illustrated in Fig. 4-12 through Fig. 4-14.



**Figure 4-12. I2S Format**



**Figure 4-13. Left/Right Justified Format**



**Figure 4-14. TDM Format**

### 4.5.3 Phase Alignment

The phase-alignment function can be used to ensure the BCLK and FSYNC outputs are phase-aligned to the CLK\_IN frequency reference. The function can be triggered manually using a control-register write, or automatically based on a configurable phase-offset threshold.

Phase alignment is enabled using [PHASE\\_ALIGNMENT\\_EN](#). If this bit is set, the CS2600 monitors the phase offset between the FSYNC output and CLK\_IN reference. For correct operation, the CLK\_IN frequency must be less than 1 MHz, and the FSYNC frequency must be equal to, or an integer multiple of, CLK\_IN frequency.

Phase alignment supports automatic or manual triggering; the applicable behavior is selected using [PHASE\\_ALIGNMENT\\_MODE](#).

- If manual trigger is selected, the phase-alignment process is triggered by writing 1 to [PHASE\\_ALIGNMENT\\_TRIG](#).
- If automatic trigger is selected, the phase-alignment process is triggered whenever the detected phase offset between CLK\_IN and FSYNC exceeds the threshold configured using [PHASE\\_ALIGNMENT\\_THR](#).

An optional phase-stability monitor can also be used to gate the automatic phase-alignment process. If [PHASE\\_ALIGNMENT\\_STB\\_EN](#) is set, the phase stability is analyzed, and the phase alignment is only implemented if the phase offset is stable. Enabling the phase-stability monitor allows a lower phase-alignment threshold to be configured without erroneous trigger conditions.

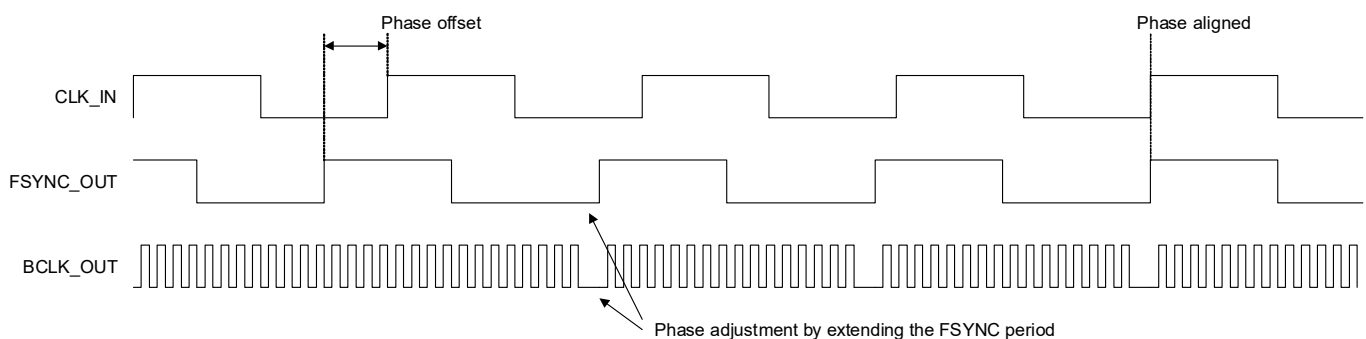
Note that phase alignment is only supported if the PLL is frequency locked. If the trigger condition (manual or automatic) is detected and the PLL is not locked, the trigger is queued until frequency lock is achieved—phase alignment is applied after the PLL frequency-unlock indicator ([F\\_UNLOCK](#)) is cleared.

If a valid trigger condition is detected, the phase of the FSYNC and BCLK outputs is adjusted in order to restore the phase alignment. The phase is adjusted by extending the FSYNC clock period by a fixed amount, and maintaining this extended period until the phase offset is corrected. The maximum permitted extension of the FSYNC clock period is selected using [PHASE\\_ALIGNMENT\\_SPEED](#); this controls how quickly the phase adjustment is implemented.

Note that, once the phase-alignment process has started, it runs to completion based on the initial phase-offset measurement, regardless of any subsequent changes in the CLK\_IN phase. If the phase offset on completion exceeds the automatic-trigger threshold, or a new manual trigger is applied, the process starts again.

Additional guidance on configuring the phase-alignment function is provided in [Section 5.2](#).

The phase-alignment process is illustrated in [Fig. 4-15](#).



**Figure 4-15. Phase Alignment**

#### 4.5.3.1 CLK\_IN Phase Selection

Phase alignment ensures the start of an FSYNC period aligns with a transition of the CLK\_IN signal. (Note that not every FSYNC period aligns with a CLK\_IN transition—this depends upon the ratio of the two frequencies.)

The FSYNC period starts on a rising edge ( $\text{FSYNC\_INV} = 0$ ) or falling edge ( $\text{FSYNC\_INV} = 1$ ). The FSYNC period is aligned to a rising or falling CLK\_IN transition as follows:

- If  $\text{CLK\_IN\_INV} = 0$ , the FSYNC period aligns with a rising CLK\_IN edge.
- If  $\text{CLK\_IN\_INV} = 1$ , the FSYNC period aligns with a falling CLK\_IN edge.

Note that, for each of the typical digital-audio formats described in Table 4-3, the  $\text{CLK\_IN\_INV}$  bit should be set to the same value as  $\text{FSYNC\_INV}$ .

### 4.5.3.2 Phase Alignment Indication

The phase-alignment status is indicated using  $\text{P\_UNLOCK}$ . This bit is set if the phase offset between FSYNC and CLK\_IN exceeds the automatic-trigger threshold (including if the PLL is disabled or is not frequency locked). The bit is also set if the phase alignment is in progress (i.e., triggered but not yet complete). The phase-alignment status can be indicated on an auxiliary output pin as described in Section 4.6. The status can be used to automatically disable the clock outputs—see Section 4.5.4 for further details.

The phase-alignment status is also indicated using  $\text{P\_UNLOCK\_STICKY}$ . This is a latching bit—it is set when  $\text{P\_UNLOCK}$  is set, and remains set until a 1 is written to the bit. Note the bit cannot be cleared if  $\text{P\_UNLOCK}$  is set.

### 4.5.4 Clock-Stop Logic

The clock output signals are valid if the PLL is enabled and locked. The clock signals are not valid if the PLL is not locked. If phase alignment is important for the target application, the clock signals may be considered invalid if the phase offset exceeds the required tolerance.

To avoid spurious clock generation, the  $\text{OUT\_GATE}$  bit can be used to stop the outputs whenever the PLL is not locked. If  $\text{OUT\_GATE} = 0$ , the clock outputs are stopped automatically if they are not valid. The  $\text{OUT\_GATE\_TYPE}$  field selects the logic condition used to determine whether the outputs are valid.

- If  $\text{OUT\_GATE\_TYPE} = 10$ , the clock outputs are gated by the analog-PLL lock status. The outputs are enabled if the analog PLL is locked to the timing reference.
- If  $\text{OUT\_GATE\_TYPE} = 00$ , the clock outputs are gated by the PLL frequency-lock status ( $\text{F\_UNLOCK}$ ). The outputs are enabled if the hybrid PLL (analog PLL and digital FLL) is frequency locked.

Note that, if the FLL is not used (e.g., in Synthesizer Mode), the outputs are gated by the analog-PLL lock status.

- If  $\text{OUT\_GATE\_TYPE} = 01$ , the clock outputs are gated by the PLL phase-alignment status ( $\text{P\_UNLOCK}$ ). The outputs are enabled if the hybrid PLL is frequency locked and phase aligned with the frequency reference.

Note that, if phase alignment is disabled, the outputs are gated by the frequency-lock status.

If the clock outputs are stopped as a result of the PLL lock or phase-alignment status, the CS2600 controls the signals to ensure there are no partial clock periods—the outputs are stopped at the end of a complete FSYNC period.

**Notes:** By default, the FSYNC period starts on a rising edge of the FSYNC signal. If FSYNC is inverted ( $\text{FSYNC\_INV} = 1$ ), the FSYNC period starts on a falling edge of FSYNC.

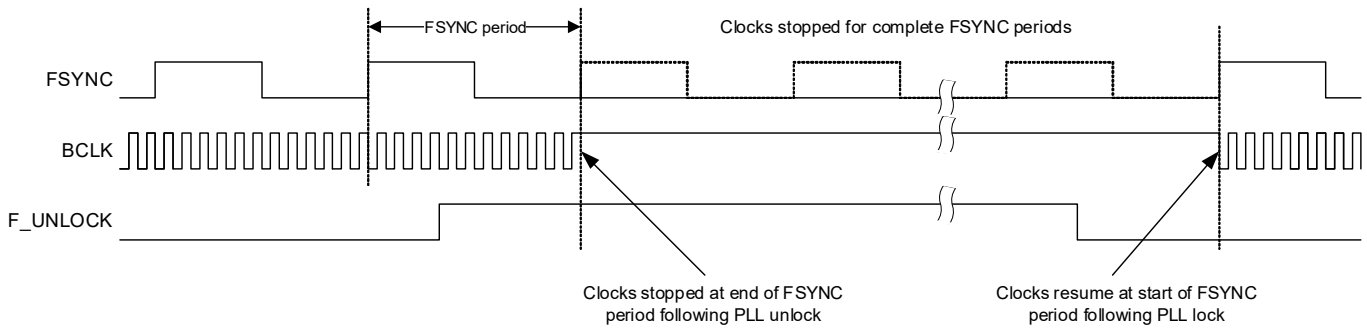
If the BCLK rate is a non-integer division of the FSYNC rate, the outputs are stopped at the end of a complete FSYNC frame that coincides with a BCLK edge.

The stopped clocks are Logic 0 if non-inverted, or Logic 1 if inverted. See Section 4.5.1 and Section 4.5.2 to invert the respective clock outputs.

The CS2600 maintains the timing of the FSYNC periods while the clocks are stopped. The timing is referenced to the CLK\_IN signal prior to the clock-stop condition occurring. When the applicable conditions (see  $\text{OUT\_GATE\_TYPE}$ ) allow the clocks to be enabled, the clocks resume at the start of the next FSYNC period.



The clock-stop timing is illustrated in Fig. 4-16. In the example shown FSYNC is noninverted, BCLK is inverted.



**Figure 4-16. Clock-Stop Timing**

If the PLL is disabled, the clock outputs are stopped immediately; the stopped CLK\_OUT, FSYNC\_OUT, and BCLK\_OUT signals can be either Logic 0 or Logic 1. Note that the clock outputs are initialized during PLL enable (Logic 0 if non-inverted, or Logic 1 if inverted), prior to starting the clock output; the timing is controlled to ensure there are no partial clock periods.

The clock-output logic is described in Table 4-4. The CLK\_OUT, FSYNC\_OUT, and BCLK\_OUT clocks are configured using the respective control fields.

**Table 4-4. Clock Output Logic—CLK\_OUT, FSYNC\_OUT, BCLK\_OUT**

| x_OUT_DIS | PLL Enable | OUT_GATE | OUT_GATE_TYPE | F_UNLOCK | P_UNLOCK | APLL unlock Status | x_OUT_INV    | x_OUT pin    |   |
|-----------|------------|----------|---------------|----------|----------|--------------------|--------------|--------------|---|
| 1         | —          | —        | —             | —        | —        | —                  | —            | Hi-Z         |   |
| 0         | Disabled   | 0        | 00            | —        | —        | —                  | —            | 0 or 1       |   |
|           |            |          |               | 0        | —        | —                  | —            | Clock output |   |
|           | 1          |          |               | —        | —        | 0                  | 0            |              |   |
|           | —          |          |               | —        | —        | 1                  | 1            |              |   |
|           | —          |          |               | 0        | —        | —                  | Clock output |              |   |
|           | —          |          |               | 1        | —        | —                  | 0            | 0            |   |
|           | Enabled    |          | 01            | —        | —        | —                  | —            | 1            | 1 |
|           |            |          |               | —        | —        | —                  | —            | 0            | 0 |
|           |            |          | 10            | —        | —        | Locked             | —            | Clock output |   |
|           |            |          |               | —        | —        | Unlocked           | 0            | 0            |   |
| 1         | —          | —        | —             | —        | —        | 1                  | 1            |              |   |
| 1         | —          | —        | —             | —        | —        | —                  | Clock output |              |   |

**Notes:**

- If the clocks are stopped due to PLL frequency/phase unlock, the clocks are stopped at the end of the FSYNC period.
- The CLK\_OUT signal is not affected by the clock-stop logic if ALTCLK is selected as the clock source.

## 4.6 Auxiliary Output

The CS2600 supports two auxiliary outputs with selectable functionality. The AUX1\_OUT pin can be configured as a clock or status output using AUX1\_OUT\_SEL. The supported functions for the AUX1 output are:

- Timing reference clock (REF\_CLK\_IN or internal oscillator)
- Frequency reference clock (CLK\_IN)
- Output clock (CLK\_OUT)
- PLL frequency-lock status (asserted if PLL is not frequency locked)
- Phase-alignment status (asserted if phase alignment is not locked)
- BCLK
- FSYNC
- Frequency reference (CLK\_IN) status (asserted if CLK\_IN is not present)

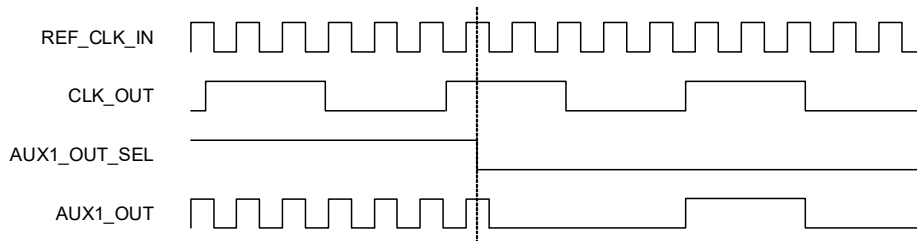


The second auxiliary output is supported on the SPI\_SDO/AUX2\_OUT/CONFIG5 pin. The AUX2\_OUT function is enabled and configured using [AUX2\\_OUT\\_SEL](#). The supported functions for the AUX2 output are:

- PLL frequency-lock status (asserted if PLL is not frequency locked)
- Phase-alignment status (asserted if phase alignment is not locked)
- Frequency reference (CLK\_IN) status (asserted if CLK\_IN is not present)

**Note:** If the AUX2\_OUT function is enabled, the SPI\_SDO function is not supported. In this configuration, the SPI interface supports write operations only.

A glitchless transition is provided if the auxiliary output is switched between the timing reference and CLK\_OUT, ensuring there are no partial clock periods in the output signal. The glitchless transition is illustrated in [Fig. 4-17](#).



**Figure 4-17. Glitchless Transition between Clock Signals**

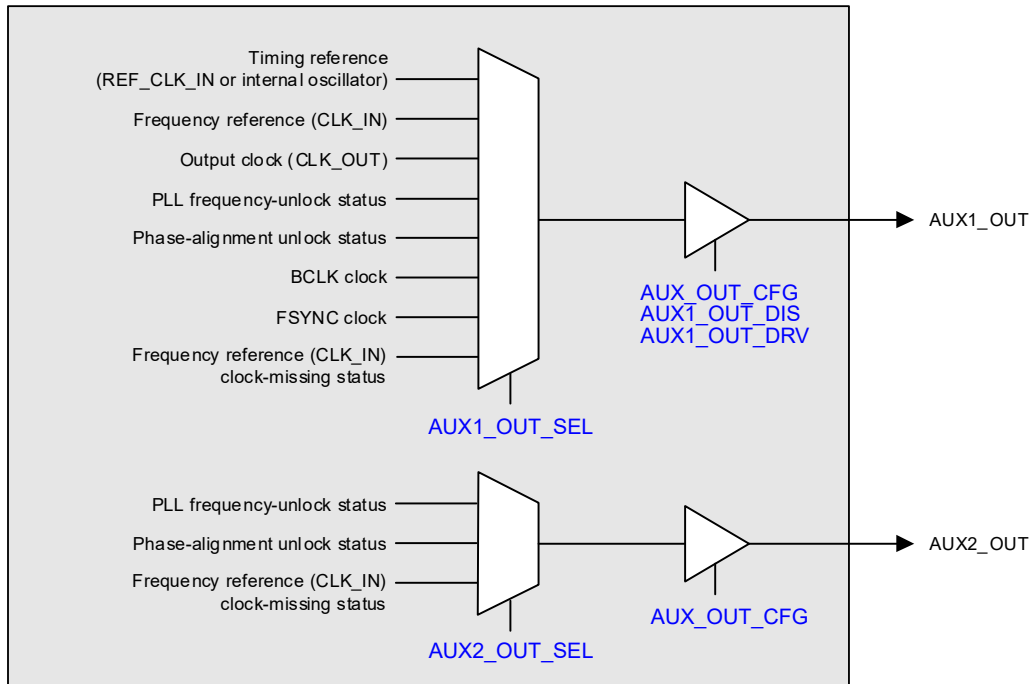
If an auxiliary output is configured as an unlock or clock-missing status, the respective output driver can be configured as either CMOS (active high) or open drain (active low). The output drivers are configured using [AUX\\_OUT\\_CFG](#).

**Note:** If the auxiliary output is configured as a clock output, the output driver is CMOS in all cases.

The AUX1 output driver can be enabled using [AUX1\\_OUT\\_DIS](#). If the AUX1 output is disabled, the driver is configured in a high-impedance (Hi-Z) state. The AUX1 drive strength is configurable using [AUX1\\_OUT\\_DRV](#).

**Note:** The [AUX1\\_OUT\\_DIS](#) field must not be updated at the same time as [AUX1\\_OUT\\_SEL](#) (at the same register address). To update both fields, a separate control-interface transaction must be scheduled for each bit.

The auxiliary outputs are illustrated in Fig. 4-18.



**Figure 4-18. Auxiliary Output Configuration**

## 4.7 I<sup>2</sup>C/SPI Control Port

The CS2600 incorporates a control port, supporting I<sup>2</sup>C or SPI modes of operation. In Software Control Mode, the CS2600 is configured by writing to control registers using the control port.

The control port is configured in I<sup>2</sup>C mode or SPI mode using the I2C\_ADDR/  $\overline{\text{SPI\_CS}}$  pin.

- I<sup>2</sup>C mode is selected by connecting the I2C\_ADDR/  $\overline{\text{SPI\_CS}}$  pin to VDD or GND using a pull-up or pull-down resistor. The pin connection is used to select the target address on the I<sup>2</sup>C bus.
- SPI mode is selected by a high-to-low transition on the I2C\_ADDR/  $\overline{\text{SPI\_CS}}$  pin after power-on.

### 4.7.1 I<sup>2</sup>C Interface

The I<sup>2</sup>C control port is supported using the I2C\_SCL and I2C\_SDA pins.

The CS2600 is a target device on the I<sup>2</sup>C bus—SCL is a clock input, SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS2600 transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit target address (this is not the same as the address of each register in the register map). Note that the LSB of the target address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I<sup>2</sup>C target address is configured using the I2C\_ADDR/SPI\_CS pin as described in [Table 4-5](#).

**Table 4-5. I<sup>2</sup>C Target Address Selection**

| I2C_ADDR Pin Connection |        | I <sup>2</sup> C Address  |
|-------------------------|--------|---------------------------|
| Pull-up to VDD          | 0 Ω    | 0x5E (write), 0x5F (read) |
|                         | 4.7 kΩ | 0x5C (write), 0x5D (read) |
|                         | 22 kΩ  | 0x5A (write), 0x5B (read) |
|                         | 100 kΩ | 0x58 (write), 0x59 (read) |
| Pull-down to GND        | 100 kΩ | 0x56 (write), 0x57 (read) |
|                         | 22 kΩ  | 0x54 (write), 0x55 (read) |
|                         | 4.7 kΩ | 0x52 (write), 0x53 (read) |
|                         | 0 Ω    | 0x50 (write), 0x51 (read) |

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS2600 responds to the start condition and shifts in the next eight bits on SDA (8-bit target address, including read/write bit, MSB first). If the target address received matches the target address of The CS2600, it responds by pulling SDA low on the next clock pulse (ACK). If the target address is not recognized, the CS2600 returns to the idle condition and waits for a new start condition.

If the target address matches the target address of the CS2600, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence, the CS2600 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

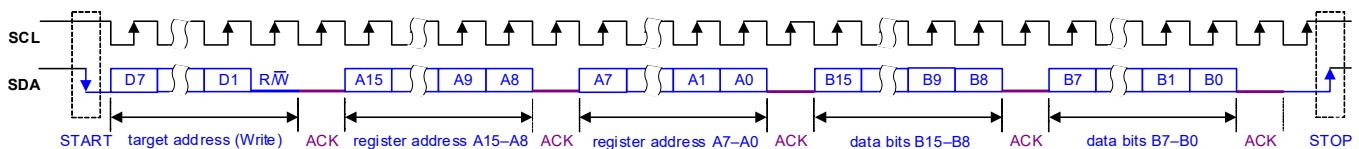
The I<sup>2</sup>C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). Note that the full I<sup>2</sup>C message protocol also includes a target address, a read/write bit, and other signaling bits (see [Fig. 4-19](#) and [Fig. 4-20](#)).

The CS2600 supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS2600 automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

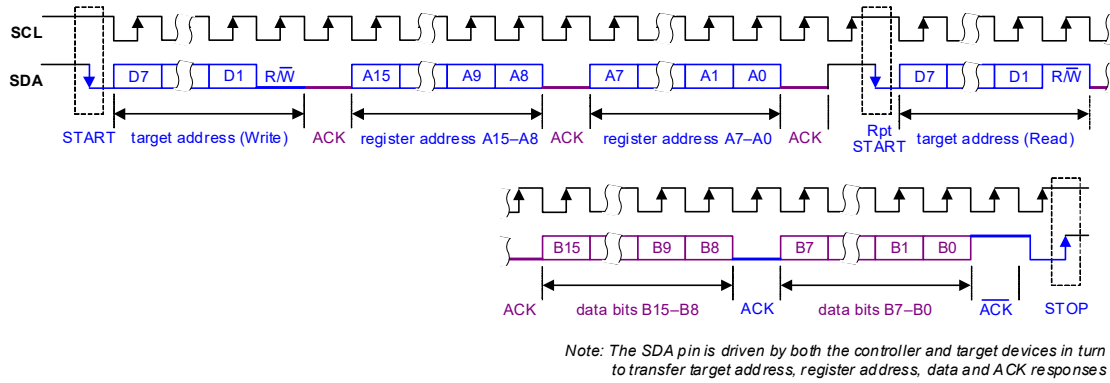
The I<sup>2</sup>C protocol for a single, 16-bit register write operation is shown in [Fig. 4-19](#).



*Note: The SDA pin is used as input for the control register address and data; SDA is pulled low by the receiving device to provide the acknowledge (ACK) response*

**Figure 4-19. Control Interface I<sup>2</sup>C Register Write**

The I<sup>2</sup>C protocol for a single, 16-bit register read operation is shown in Fig. 4-20.



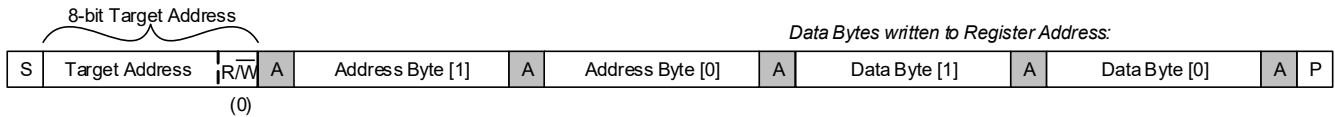
**Figure 4-20. Control Interface I<sup>2</sup>C Register Read**

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-21 through Fig. 4-24. The terminology used in the following figures is detailed in Table 4-6.

**Table 4-6. Control Interface (I<sup>2</sup>C) Terminology**

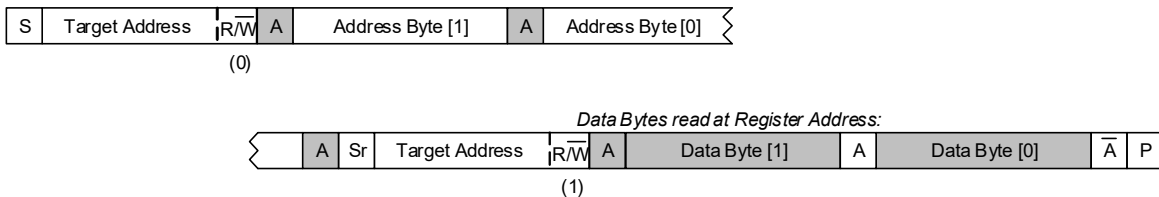
| Terminology   | Description                             |
|---------------|---|
| S             | Start condition                         |
| Sr            | Repeated start                          |
| A             | Acknowledge (SDA low)                   |
| $\bar{A}$     | No Acknowledge (SDA high)               |
| P             | Stop condition                          |
| R/W           | Read/not Write: 0 = Write, 1 = Read     |
| [White field] | Data flow from bus controller to CS2600 |
| [Gray field]  | Data from CS2600 to bus controller      |

Fig. 4-21 shows a single register write to a specified address.



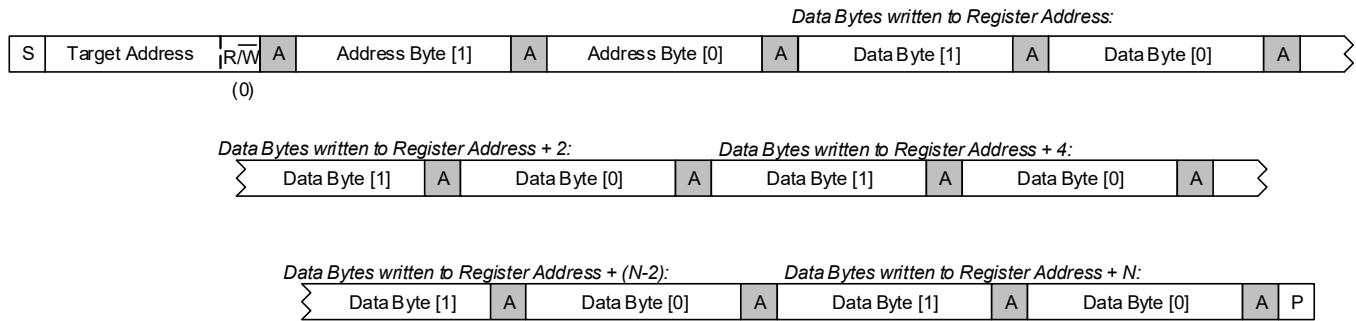
**Figure 4-21. Single-Register Write to Specified Address**

Fig. 4-22 shows a single register read from a specified address.



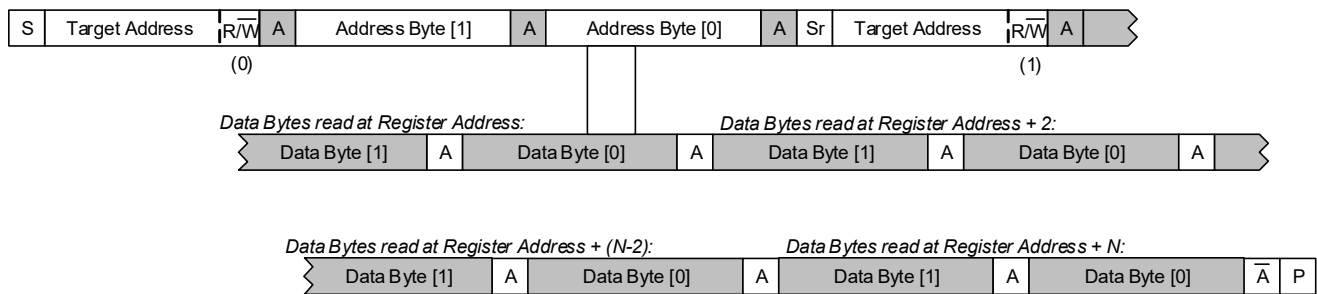
**Figure 4-22. Single-Register Read from Specified Address**

Fig. 4-23 shows a multiple register write to a specified address.



**Figure 4-23. Multiple-Register Write to Specified Address**

Fig. 4-24 shows a multiple register read from a specified address.



**Figure 4-24. Multiple-Register Read from Specified Address**

## 4.7.2 SPI Interface

The SPI interface is supported using the  $\overline{\text{SPI\_CS}}$ , SPI\_SCK, SPI\_SDI, and SPI\_SDO pins.

The  $\overline{\text{SPI\_CS}}$  pin provides the chip-select input (active low). Data is clocked in/out on the rising edge of SPI\_SCK.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/W = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/W = 1), the SDI pin is ignored following receipt of the valid register address.

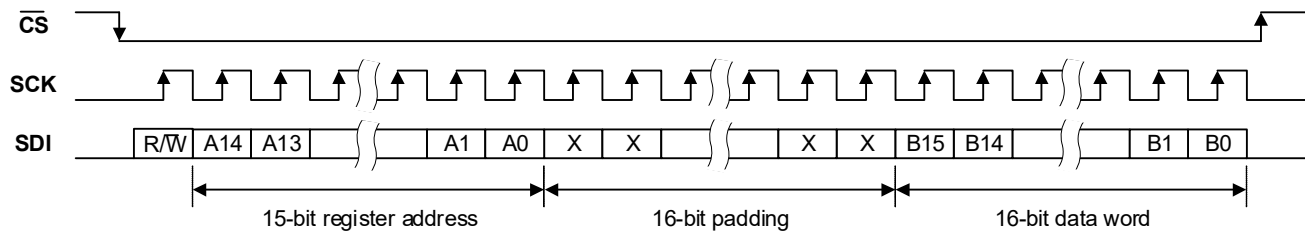
The SDO (data-output) pin supports the following behavior:

- If  $\overline{\text{CS}}$  is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If  $\overline{\text{CS}}$  is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-6 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. Note that the full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-25 and Fig. 4-26).

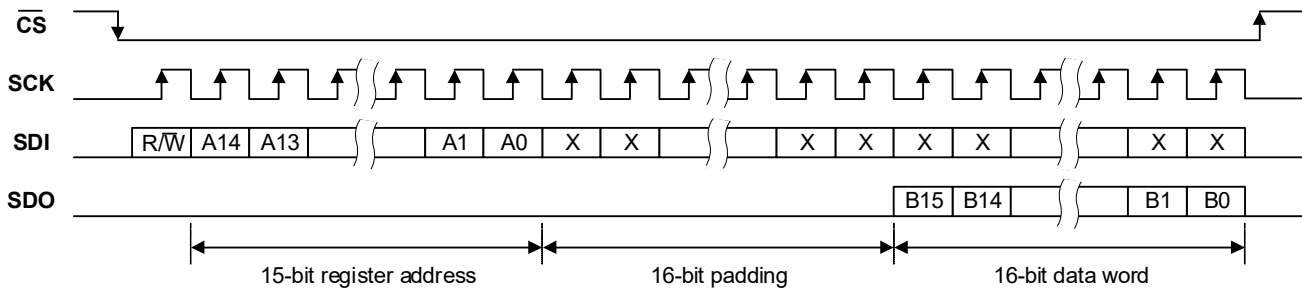
Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS2600 automatically increments the register address at the end of each data word, for as long as  $\overline{\text{CS}}$  is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

Fig. 4-25 shows a single register write to a specified address.



**Figure 4-25. Control Interface SPI Register Write**

Fig. 4-26 shows a single register read from a specified address.



**Figure 4-26. Control Interface SPI Register Read**

### 4.7.3 Device Configuration

The device should be fully configured before enabling the PLL. When changing any register settings, it is recommended to disable the PLL, update the registers, then enable the PLL; this ensures there is no unintended behavior.

See [Section 4.3.1](#) to enable and disable the PLL. Specific restrictions and exceptions on updating register fields are described in [Section 4.7.3.2](#).

#### 4.7.3.1 Freezable Fields

The register map supports a number of freezable fields, as listed in [Table 4-7](#). If `FREEZE_EN` is set, these fields are frozen to their current values regardless of any register writes. If a new value is written, the value is buffered and does not become effective until `FREEZE_EN` is cleared. When `FREEZE_EN` is cleared, all of the frozen fields become active simultaneously.

**Note:** The `FREEZE_EN` bit should not be updated in the same write transaction as the freezable fields `PLL_MODE_SEL` or `M_RATIO_SEL` at the same register address. Separate write transactions should be used to ensure the correct sequencing of the freeze function.

**Table 4-7. Freezable Fields**

| Address | Fields   |
|---------|--|
| 0x0002  | <a href="#">CLK_OUT_DIS</a> , <a href="#">AUX1_OUT_DIS</a> , <a href="#">S_RATIO_SEL</a> , <a href="#">RATIO_MOD</a> |
| 0x0004  | <a href="#">PLL_MODE_SEL</a> , <a href="#">M_RATIO_SEL</a>   |
| 0x0100  | <a href="#">FSYNC_OUT_DIS</a> , <a href="#">BCLK_OUT_DIS</a>   |
| 0x0102  | <a href="#">AUX1_OUT_SEL</a>   |

### 4.7.3.2 Field Update Restrictions

The fields listed in [Table 4-8](#) can be configured at any time, and do not result in any partial clock period in the outputs.

**Table 4-8. Register Fields with No Write Restrictions**

| Address       | Fields  |
|---------------|---|
| 0x0002        | <a href="#">CLK_OUT_DIS</a> , <a href="#">AUX1_OUT_DIS</a> <sup>1</sup> , <a href="#">PLL_EN1</a> |
| 0x0004        | <a href="#">PLL_EN2</a> , <a href="#">FREEZE_EN</a>   |
| 0x0100        | <a href="#">FSYNC_OUT_DIS</a> , <a href="#">BCLK_OUT_DIS</a>                                      |
| 0x0102        | <a href="#">AUX1_OUT_SEL</a>  |
| 0x0114        | <a href="#">F_UNLOCK_STICKY</a> , <a href="#">P_UNLOCK_STICKY</a>                                 |
| 0x0116        | <a href="#">ERR_STS1</a> – <a href="#">ERR_STS8</a>   |
| 0x0120        | <a href="#">OTP_LDO_EN</a> , <a href="#">OTP_LDO_DISCH_EN</a> , <a href="#">OTP_VDD_EN</a>        |
| 0x1104        | <a href="#">USER_KEY</a>  |
| 0x2340–0x236E | <a href="#">OTP_IMG_WR_BYTE1</a> – <a href="#">OTP_IMG_WR_BYTE48</a>                              |
| 0x2400        | <a href="#">OTP_PROG_EN</a>   |

1. Note the [AUX1\\_OUT\\_DIS](#) field must not be updated at the same time as [AUX1\\_OUT\\_SEL](#). See [Section 4.6](#).

The fields listed in [Table 4-9](#) can be configured at any time, but may cause the PLL to lose lock temporarily.

**Table 4-9. Register Fields with Restrictions**

| Address       | Fields  |
|---------------|---|
| 0x0002        | <a href="#">S_RATIO_SEL</a> <sup>1</sup> , <a href="#">RATIO_MOD</a>    |
| 0x0004        | <a href="#">PLL_MODE_SEL</a> , <a href="#">M_RATIO_SEL</a> <sup>1</sup> |
| 0x0006–0x0008 | <a href="#">RATIO1_1</a> , <a href="#">RATIO1_2</a>                     |
| 0x000A–0x000C | <a href="#">RATIO2_1</a> , <a href="#">RATIO2_2</a>                     |
| 0x000E–0x0010 | <a href="#">RATIO3_1</a> , <a href="#">RATIO3_2</a>                     |
| 0x0012–0x0014 | <a href="#">RATIO4_1</a> , <a href="#">RATIO4_2</a>                     |
| 0x0016        | <a href="#">REF_CLK_IN_DIV</a> , <a href="#">RATIO_CFG</a>              |

1. The [S\\_RATIO\\_SEL](#) and [M\\_RATIO\\_SEL](#) fields can be configured at any time, provided the respective field values differ from each other before the update and after the update. In all other cases, the PLL should be disabled before writing to either of these fields.

Note that, for all other control fields (not listed in [Table 4-8](#) or [Table 4-9](#)), the PLL should be disabled before reconfiguring; failure to do so may result in unintended behavior, and may require a software reset to restart the device.

### 4.7.4 Software Reset

A software reset is triggered by writing 0x5A to the [SW\\_RST](#) field. A software reset causes all of the CS2600 control registers to be reset to their default states.

### 4.7.5 Power-On Reset

The power-on reset (POR) sequence is scheduled on initial power-up, and following any interruption to the VDD supply. The POR causes all of the CS2600 control registers to be reset to their default states.

## 4.8 One-Time Programmable (OTP) Memory

The CS2600 incorporates a customer-programmable OTP memory which can be used to automatically configure the device after power-up. The OTP memory enables the device to be factory programmed for a specific target application, removing the need for a host system to configure the device.

The OTP memory is programmed using the I<sup>2</sup>C or SPI interface. The CS2600 supports two different OTP programming methods, for production and prototyping respectively. A device may be programmed using either method, but not both.

- Production programming ensures data integrity using an error correction code (ECC) algorithm.
- Prototype programming provides greater flexibility to reprogram the device during product development.

Note that the OTP memory contents have no effect if the CS2600 is used in Hardware Control Mode.

### 4.8.1 OTP Programming Supply

An OTP programming supply (VDD\_OTP) is required when writing to the OTP memory. The programming supply may be provided internally or externally, depending on the system supply (VDD).

- If the VDD supply is 3.3 V, the programming supply can be provided using an internal LDO regulator; in this case, the output of the regulator, VLDO\_OTP, should be connected to VDD\_OTP.
- If the VDD supply is 1.8 V, the programming supply must be provided externally.

The external connections for the OTP programming supply are shown in [Fig. 2-1](#).

**Note:** VDD must be present before enabling the VDD\_OTP pin. The external VDD\_OTP supply must be removed before powering down VDD.

### 4.8.2 Production Programming

Production programming is implemented using an image that defines the required settings of all the configurable registers. The image is generated using SoundClear Studio (SCS).

The image includes an ID field (1–7) and an error correction code (ECC) field. The ECC supports 3-bit error detection and 2-bit error correction.

The programmed contents of the OTP memory are loaded during startup. If the OTP memory contains an uncorrectable error, the clock outputs are disabled and the device startup is aborted. An OTP error is indicated using [ERR\\_STS7](#).

The OTP memory can be programmed up to seven times. Each time the OTP memory is programmed, the previous images are automatically superseded.

### 4.8.3 Prototype Programming

Prototype programming is used to fine-tune the device settings for a specific application. The prototype programming configures selected fields only, with all other fields initializing to their respective default values.

Prototype programming is configured using SoundClear Studio (SCS). The programmed contents of the OTP memory are loaded during startup. Note there is no error checking when using the prototype programming option.

Iterative programming is supported, with modified values defined for specific fields. If a field is programmed multiple times in the OTP memory, the most recent programmed value is applied during startup.

The OTP memory can be programmed multiple times. The programming limit depends on which parameters are being configured. As an example, however, it is possible to program and modify the PLL ratio more than 25 times.



## 4.9 Hardware Control Mode

The CS2600 supports hardware and software control modes. In Hardware Control Mode, the device configuration is determined by external resistors connected to the hardware-control pins, CONFIG1–CONFIG6. The external resistors are connected to GND or VDD; different resistor values allow the CS2600 to detect eight configuration options per pin. Note that the external resistance must be within 5% of the specified value.

Hardware Control Mode is selected using an external resistor connected to CONFIG1. In Hardware Control Mode, the PLL is enabled in Synthesizer Mode or Multiplier Mode as specified in [Table 4-11](#). Software Control Mode (I<sup>2</sup>C/SPI) is selected by connecting CONFIG1 to GND.

In Hardware Control Mode, the device configuration is latched during the power-up sequence and cannot be changed while the device is operational. To update the device configuration, the device must be power cycled in order to read new settings on the CONFIGx pins.

If an invalid hardware configuration is selected, the clock outputs are disabled. Normal operation resumes when a valid configuration is detected. Note that a valid configuration may depend on the external clocks (e.g., CLK\_IN frequency).

The CONFIG pins provide control over a subset of the overall device functionality. For the remaining functions, the respective default settings are applied. A summary of the CONFIG pin functions is shown in [Table 4-10](#).

**Table 4-10. CONFIG Pin Summary**

| CONFIG Pin | Description                                   |
|------------|---|
| CONFIG1    | PLL Operating Mode and Timing Clock Reference |
| CONFIG2    | Holdover Mode, PLL bandwidth, and AUX1 output |
| CONFIG3    | Clock output                                  |
| CONFIG4    | BCLK frequency                                |
| CONFIG5    | Automatic Rate Control and FSYNC frequency    |
| CONFIG6    | CLK_OUT frequency                             |

The CONFIG1 pin selects the PLL operating mode and the timing-reference clock frequency as shown in [Table 4-11](#).

**Table 4-11. CONFIG1 Hardware Configuration**

| Pin Configuration |        | Operating Mode                               | Timing Reference Frequency <sup>1</sup> |
|-------------------|--------|--|---|
| Pull-up to VDD    | 0 Ω    | Synthesizer                                  | 10 MHz                                  |
|                   | 4.7 kΩ |  | 25 MHz                                  |
|                   | 22 kΩ  |  | 24.576 MHz                              |
|                   | 100 kΩ |  | 49.152 MHz                              |
| Pull-down to GND  | 100 kΩ | Multiplier                                   | 8–18 MHz                                |
|                   | 22 kΩ  |  | 16–37.5 MHz                             |
|                   | 4.7 kΩ |  | 32–75 MHz                               |
|                   | 0 Ω    | Software Control Mode (I <sup>2</sup> C/SPI) |   |

1. The timing reference can be REF\_CLK\_IN, external crystal oscillator (XTAL\_IN), or the internal oscillator (LCO). In Hardware Mode, the internal oscillator is supported for Multiplier Mode only.

In Multiplier Mode, the remaining CONFIGx pin functions are described in [Section 4.9.1](#).

In Synthesizer Mode, the remaining CONFIGx pin functions are described in [Section 4.9.2](#).

### 4.9.1 Multiplier Mode

The CONFIG2 pin selects Holdover Mode, PLL bandwidth, and the AUX1\_OUT function as shown in [Table 4-12](#).

**Table 4-12. CONFIG2 Hardware Configuration—Multiplier Mode**

| Pin Configuration |        | Holdover Mode | PLL Bandwidth | AUX1 Output                |
|-------------------|--------|---------------|---------------|----------------------------|
| Pull-up to VDD    | 0 Ω    | Enabled       | 1 Hz          | Frequency Unlock Indicator |
|                   | 4.7 kΩ |               |               | Phase Unlock Indicator     |
|                   | 22 kΩ  |               | 128 Hz        | Frequency Unlock Indicator |
|                   | 100 kΩ |               |               | Phase Unlock Indicator     |
| Pull-down to GND  | 100 kΩ | Disabled      | 1 Hz          | Phase Unlock Indicator     |
|                   | 22 kΩ  |               |               | Frequency Unlock Indicator |
|                   | 4.7 kΩ |               | 128 Hz        | Phase Unlock Indicator     |
|                   | 0 Ω    |               |               | Frequency Unlock Indicator |

The CONFIG3 pin selects the clock output configuration as shown in [Table 4-13](#). The supported configurations are designed for target applications using I<sup>2</sup>S, LJ/RJ, or TDM serial data interfaces.

**Table 4-13. CONFIG3 Hardware Configuration—Multiplier Mode**

| Pin Configuration |        | Phase Alignment | Target Application | Input/Output Configuration |              |                        |
|-------------------|--------|-----------------|--------------------|----------------------------|--------------|------------------------|
|                   |        |                 |                    | CLK_IN                     | BCLK_OUT     | FSYNC_OUT <sup>1</sup> |
| Pull-up to VDD    | 0 Ω    | Enabled         | I <sup>2</sup> S   | Inverted                   | Inverted     |                        |
|                   | 4.7 kΩ |                 | LJ/RJ              | Not Inverted               | Inverted     | Not Inverted           |
|                   | 22 kΩ  |                 | TDM-A <sup>2</sup> |                            |              |                        |
|                   | 100 kΩ |                 | TDM-B <sup>2</sup> |                            |              |                        |
| Pull-down to GND  | 100 kΩ | Disabled        | I <sup>2</sup> S   |                            | Inverted     |                        |
|                   | 22 kΩ  |                 | LJ/RJ              | Inverted                   | Not Inverted |                        |
|                   | 4.7 kΩ |                 | TDM-A <sup>2</sup> |                            |              |                        |
|                   | 0 Ω    |                 | TDM-B <sup>2</sup> |                            |              |                        |

1. In TDM applications, the FSYNC duty cycle corresponds to 1 BCLK period. In other formats, the FSYNC duty cycle is 50%.

2. The TDM-A and TDM-B selections provide the same inverted/non-inverted behavior. The two options differ from each other in how the BCLK frequency is determined, as described in [Table 4-14](#).

The CONFIG4 pin selects the BCLK output frequency as shown in [Table 4-14](#). Note the pin function is dependent on the target application (see CONFIG3 pin configuration in [Table 4-13](#)).

**Table 4-14. CONFIG4 Hardware Configuration—Multiplier Mode**

| Pin Configuration |        | BCLK Frequency   |                                    |              |              |
|-------------------|--------|------------------|------------------------------------|--------------|--------------|
|                   |        | I <sup>2</sup> S | Left-Justified/<br>Right-Justified | TDM-A        | TDM-B        |
| Pull-up to VDD    | 0 Ω    | Invalid          |                                    |              |              |
|                   | 4.7 kΩ |                  |                                    |              |              |
|                   | 22 kΩ  |                  |                                    |              |              |
|                   | 100 kΩ |                  |                                    |              |              |
| Pull-down to GND  | 100 kΩ | 64 × FSYNC       | 64 × FSYNC                         | 1024 × FSYNC | CLK_OUT      |
|                   | 22 kΩ  |                  |                                    | 512 × FSYNC  | CLK_OUT / 2  |
|                   | 4.7 kΩ |                  |                                    | 256 × FSYNC  | CLK_OUT / 4  |
|                   | 0 Ω    |                  |                                    | 128 × FSYNC  | CLK_OUT / 8  |
|                   |        |                  |                                    | 64 × FSYNC   | CLK_OUT / 16 |

**Note:** Selecting a BCLK frequency referenced to FSYNC can result in an invalid BCLK divider value (depending on the FSYNC and MCLK\_OUT frequencies). Refer to the [BCLK\\_DIV](#) field for the supported BCLK divider ratios. If an invalid selection is made, the clock outputs are disabled; normal operation resumes when a valid configuration is detected.

The CONFIG5 pin selects the ARC function and the FSYNC output frequency as shown in [Table 4-15](#).

**Table 4-15. CONFIG5 Hardware Configuration—Multiplier Mode**

| Pin Configuration |        | Automatic Rate Control (ARC) | FSYNC Frequency |               |
|-------------------|--------|------------------------------|-----------------|---------------|
| Pull-up to VDD    | 0 Ω    | Enabled                      | CLK_IN          |               |
|                   | 4.7 kΩ |                              | CLK_OUT / 1024  |               |
|                   | 22 kΩ  |                              | CLK_OUT / 512   |               |
|                   | 100 kΩ |                              | CLK_OUT / 256   |               |
| Pull-down to GND  | 100 kΩ |                              | Disabled        | CLK_OUT / 128 |
|                   | 22 kΩ  |                              |                 | CLK_OUT / 64  |
|                   | 4.7 kΩ |                              |                 | CLK_OUT / 32  |
|                   | 0 Ω    |                              |                 | CLK_OUT / 16  |

The CONFIG6 pin selects the CLK\_OUT frequency as shown in [Table 4-16](#). Note the pin function is dependent on the ARC status (see CONFIG5 pin configuration in [Table 4-15](#)).

**Table 4-16. CONFIG6 Hardware Configuration—Multiplier Mode**

| Pin Configuration |        | CLK_OUT Frequency |                                    |
|-------------------|--------|-------------------|------------------------------------|
|                   |        | ARC Disabled      | ARC Enabled                        |
| Pull-up to VDD    | 0 Ω    | 128 × CLK_IN      | 12.288 or 11.2896 MHz <sup>1</sup> |
|                   | 4.7 kΩ | 256 × CLK_IN      | 24.576 or 22.5792 MHz <sup>1</sup> |
|                   | 22 kΩ  | 512 × CLK_IN      | 49.152 or 45.1584 MHz <sup>1</sup> |
|                   | 100 kΩ | 768 × CLK_IN      | Invalid                            |
| Pull-down to GND  | 100 kΩ | 1024 × CLK_IN     |                                    |
|                   | 22 kΩ  | 1536 × CLK_IN     |                                    |
|                   | 4.7 kΩ | 3072 × CLK_IN     |                                    |
|                   | 0 Ω    | 6144 × CLK_IN     |                                    |

1. The applicable frequency is the same base as CLK\_IN

## 4.9.2 Synthesizer Mode

The CONFIG2 pin selects the AUX1\_OUT function as shown in [Table 4-17](#).

**Table 4-17. CONFIG2 Hardware Configuration—Synthesizer Mode**

| Pin Configuration |        | AUX1 Output                |
|-------------------|--------|----------------------------|
| Pull-up to VDD    | 0 Ω    | Frequency Unlock Indicator |
|                   | 4.7 kΩ |                            |
|                   | 22 kΩ  |                            |
|                   | 100 kΩ |                            |
| Pull-down to GND  | 100 kΩ | Disabled                   |
|                   | 22 kΩ  |                            |
|                   | 4.7 kΩ |                            |
|                   | 0 Ω    |                            |

The CONFIG3 pin has no function in Synthesizer Mode; the pin should be connected to VDD or GND.

The CONFIG4 pin selects the BCLK output frequency as shown in [Table 4-18](#).

**Table 4-18. CONFIG4 Hardware Configuration—Synthesizer Mode**

| Pin Configuration |        | BCLK Frequency |
|-------------------|--------|----------------|
| Pull-up to VDD    | 0 Ω    | CLK_OUT / 16   |
|                   | 4.7 kΩ | CLK_OUT / 8    |
|                   | 22 kΩ  | CLK_OUT / 4    |
|                   | 100 kΩ | CLK_OUT / 2    |
| Pull-down to GND  | 100 kΩ | CLK_OUT        |
|                   | 22 kΩ  | Invalid        |
|                   | 4.7 kΩ |                |
|                   | 0 Ω    |                |

The CONFIG5 pin selects the FSYNC output frequency as shown in [Table 4-19](#).

**Table 4-19. CONFIG5 Hardware Configuration—Synthesizer Mode**

| Pin Configuration |        | FSYNC Frequency |
|-------------------|--------|-----------------|
| Pull-up to VDD    | 0 Ω    | Invalid         |
|                   | 4.7 kΩ | CLK_OUT / 1024  |
|                   | 22 kΩ  | CLK_OUT / 512   |
|                   | 100 kΩ | CLK_OUT / 256   |
| Pull-down to GND  | 100 kΩ | CLK_OUT / 128   |
|                   | 22 kΩ  | CLK_OUT / 64    |
|                   | 4.7 kΩ | CLK_OUT / 32    |
|                   | 0 Ω    | CLK_OUT / 16    |

The CONFIG6 pin selects the CLK\_OUT frequency as shown in [Table 4-20](#).

**Table 4-20. CONFIG6 Hardware Configuration—Synthesizer Mode**

| Pin Configuration |        | CLK_OUT Frequency |
|-------------------|--------|-------------------|
| Pull-up to VDD    | 0 Ω    | Invalid           |
|                   | 4.7 kΩ |                   |
|                   | 22 kΩ  | 11.2896 MHz       |
|                   | 100 kΩ | 12.288 MHz        |
| Pull-down to GND  | 100 kΩ | 22.5792 MHz       |
|                   | 22 kΩ  | 24.576 MHz        |
|                   | 4.7 kΩ | 45.1584 MHz       |
|                   | 0 Ω    | 49.152 MHz        |

## 4.10 Device ID

The device ID, and other associated data, can be read from the control fields listed in [Table 4-21](#).

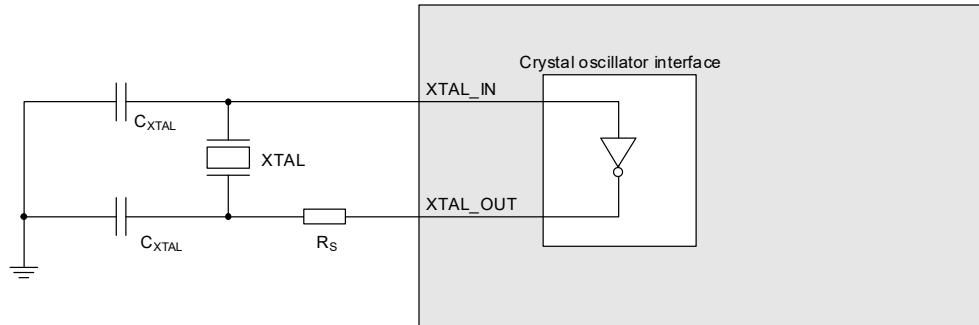
**Table 4-21. Device ID**

| Label                    | Description                 |
|--------------------------|-----------------------------|
| <a href="#">DEVID</a>    | Device ID                   |
| <a href="#">AREVID</a>   | All-layer device revision   |
| <a href="#">MTLREVID</a> | Metal-layer device revision |

## 5 Applications

### 5.1 Crystal Component Selection

The crystal oscillator (see [Section 4.2.2](#)) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in [Fig. 5-1](#). A series resistor ( $R_S$ ) may also be required to configure the drive level for the selected crystal.



**Figure 5-1. Crystal Oscillator Connection**

The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD operating voltage as described in [Table 3-4](#).

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS2600 is compatible with a wide variety of crystal components, including the NX3225SA, NX2016A, ECX-33Q, and ECX-2236Q families.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance ( $C_L$ ). The recommended value for each  $C_{XTAL}$  capacitor is  $2 \times C_L$ .
3. **Series resistor.** In the first instance, assume the series resistor  $R_S$  is not required ( $0 \Omega$ ).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor  $R_S$ , together with the crystal characteristics. If the gain margin is less than 5, a different crystal selection must be made (Step 1).

The gain margin is calculated as follows: 
$$\text{Gain Margin} = \frac{\text{Transconductance}}{4 \times (\text{ESR} + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$$

where:

Transconductance = transconductance of the crystal interface (S)

ESR = equivalent series resistance (ESR) of the crystal ( $\Omega$ )

$R_S$  = series resistance ( $\Omega$ )

$f_{XTAL}$  = resonant frequency of the crystal (Hz)

$C_L$  = load capacitance of the crystal (F)

$C_0$  = shunt capacitance of the crystal (F)

5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor  $R_S$  to meet the required specification. Increasing  $R_S$  results in a lower voltage across the crystal and a decrease in drive level.

If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

The drive level (W) is calculated as follows:  $\text{Drive Level} = 2 \times \text{ESR} \times (\pi \times f_{\text{XTAL}} \times V \times (C_L + C_0))^2$

where:

ESR = equivalent series resistance (ESR) of the crystal ( $\Omega$ )

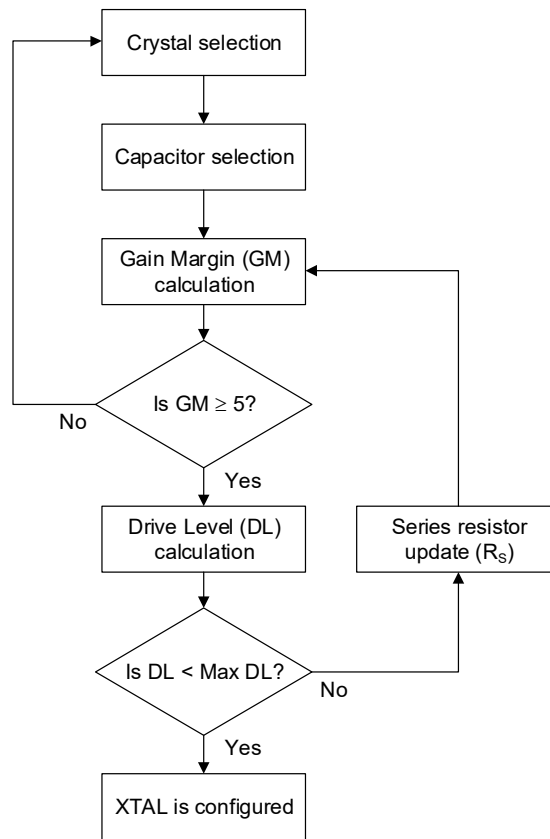
$f_{\text{XTAL}}$  = resonant frequency of the crystal (Hz)

V = Peak voltage across the crystal (V)

$C_L$  = load capacitance of the crystal (F)

$C_0$  = shunt capacitance of the crystal (F)

The sequence for crystal component selection is illustrated in [Fig. 5-2](#).



**Figure 5-2. Crystal Oscillator Component Selection**

## 5.2 Phase Alignment Configuration

The phase-alignment function (see [Section 4.5.3](#)) can be used to ensure the BCLK and FSYNC outputs are phase-aligned to the CLK\_IN frequency reference. The function can be triggered manually using a control-register write, or automatically based on a configurable phase-offset threshold.

If automatic trigger is selected, the phase-alignment process is triggered whenever the detected phase offset between CLK\_IN and FSYNC exceeds the threshold configured using [PHASE\\_ALIGNMENT\\_THR](#).

- To avoid erroneous trigger conditions, the threshold must be set higher than the expected CLK\_IN jitter. It is recommended to configure the threshold lower than the maximum acceptable phase-offset error, and at least 10 times larger than the expected peak CLK\_IN jitter.

If automatic trigger is selected, a phase-stability monitor can be used to gate the automatic phase-alignment process. If [PHASE\\_ALIGNMENT\\_STB\\_EN](#) is set, the phase stability is analyzed, and the phase alignment is only implemented if the phase offset is stable.

- The phase-stability monitor should only be enabled if the phase offset is expected to drift for some time before settling (e.g., when the CLK\_IN frequency changes).
- If the phase is unstable and [PHASE\\_ALIGNMENT\\_STB\\_EN](#) is not set, the phase alignment may be triggered multiple times; the final offset error may be larger than the specified level (see [Table 3-4](#)) and below the threshold to retrigger the phase-alignment process.

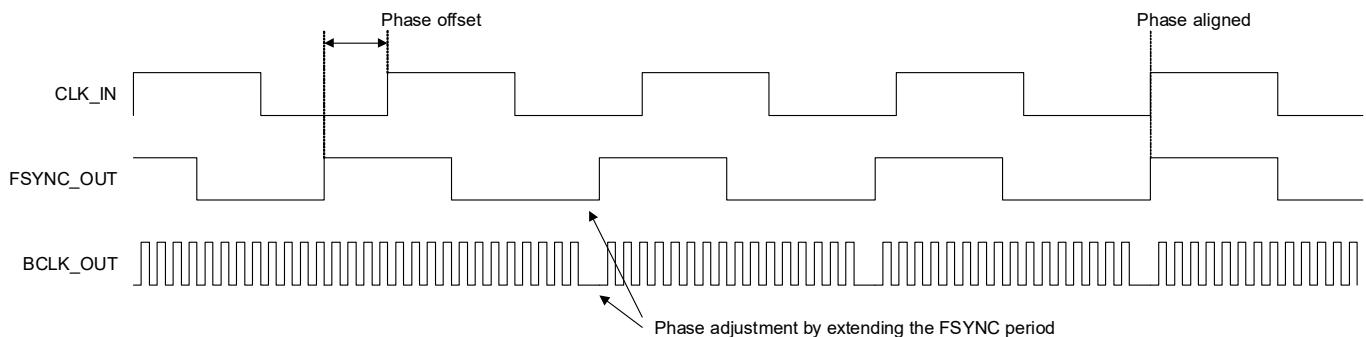
If a valid trigger condition is detected, the phase of the FSYNC and BCLK outputs is adjusted in order to restore the phase alignment. The [PHASE\\_ALIGNMENT\\_SPEED](#) field controls how quickly the phase adjustment is implemented.

- If [PHASE\\_ALIGNMENT\\_SPEED](#) = 00, the FSYNC period is extended by 1 MCLK period until the phase offset is eliminated. For example, if the initial offset is 124 MCLKs, the phase-alignment process will take 124 FSYNC periods to complete.  
In this configuration, the phase alignment is slowest, but jitter and frequency deviation is minimized.
- If [PHASE\\_ALIGNMENT\\_SPEED](#) = 01, the FSYNC period is extended by a maximum of 10 MCLK periods until the phase offset is eliminated. For example, if the initial offset is 124 MCLKs, the phase-alignment process will take 13 FSYNC periods to complete.
- If [PHASE\\_ALIGNMENT\\_SPEED](#) = 10, the FSYNC period is extended by a maximum of 50 MCLK periods until the phase offset is eliminated. For example, if the initial offset is 124 MCLKs, the phase-alignment process will take 3 FSYNC periods to complete.
- If [PHASE\\_ALIGNMENT\\_SPEED](#) = 11, the FSYNC period is extended as much as is required to complete the phase alignment in a single FSYNC period.

In this configuration, the phase alignment is fastest, but the transient FSYNC/BCLK period error may be large (depending on the size of the phase offset).

The phase-alignment speed should be configured according to the application requirements. If the output clocks are being used while the alignment is in progress, the slow rate may be chosen for optimal jitter/frequency stability. If the output clocks are not used during the alignment, the fastest rate may be preferred.

The phase-alignment process is illustrated in [Fig. 5-3](#).



**Figure 5-3. Phase Alignment**

## 6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS2600.

- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- Fields shown in orange are affected by the FREEZE bit.
- All visible fields are read/write except where indicated with the following shading:

Read/write access    
  Read-only access    
  Write-only access    
  User key password access

**Table 6-1. Block Base Addresses**

| Base Address | Block Name      | Register Quick Reference    | Register Description Reference |
|--------------|-----------------|-----------------------------|--------------------------------|
| 0x0000 0000  | <b>CONFIG</b>   | <a href="#">Section 6.1</a> | <a href="#">Section 7.1</a>    |
| 0x0000 1100  | <b>KEYS</b>     | <a href="#">Section 6.2</a> | <a href="#">Section 7.2</a>    |
| 0x0000 2000  | <b>OTP_IF</b>   | <a href="#">Section 6.3</a> | <a href="#">Section 7.3</a>    |
| 0x0000 2400  | <b>OTP_CTRL</b> | <a href="#">Section 6.4</a> | <a href="#">Section 7.4</a>    |
| 0x0000 2480  | <b>OTP_STS</b>  | <a href="#">Section 6.5</a> | <a href="#">Section 7.5</a>    |

### 6.1 CONFIG

| Address                              | Register | 15        | 14            | 13 | 12          | 11        | 10 | 9 | 8          | 7           | 6 | 5              | 4 | 3          | 2           | 1            | 0            |             |
|--------------------------------------|----------|-----------|---------------|----|-------------|-----------|----|---|------------|-------------|---|----------------|---|------------|-------------|--------------|--------------|-------------|
| 0x0000 0002<br><a href="#">p. 44</a> | PLL_CFG1 | RATIO_MOD |               |    | S_RATIO_SEL |           | —  |   | PLL_EN1    | —           |   |                |   |            |             |              | AUX1_OUT_DIS | CLK_OUT_DIS |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 1           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 0004<br><a href="#">p. 44</a> | PLL_CFG2 | —         |               |    |             | FREEZE_EN | —  |   | PLL_EN2    | —           |   |                |   |            | M_RATIO_SEL | PLL_MODE_SEL |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 1          | 0           | 0            | 0            |             |
| 0x0000 0006<br><a href="#">p. 45</a> | RATIO1_1 | RATIO1_1  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 0008<br><a href="#">p. 45</a> | RATIO1_2 | RATIO1_2  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 000A<br><a href="#">p. 45</a> | RATIO2_1 | RATIO2_1  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 000C<br><a href="#">p. 45</a> | RATIO2_2 | RATIO2_2  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 000E<br><a href="#">p. 45</a> | RATIO3_1 | RATIO3_1  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 0010<br><a href="#">p. 46</a> | RATIO3_2 | RATIO3_2  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 0012<br><a href="#">p. 46</a> | RATIO4_1 | RATIO4_1  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 0014<br><a href="#">p. 46</a> | RATIO4_2 | RATIO4_2  |               |    |             |           |    |   |            |             |   |                |   |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 0016<br><a href="#">p. 46</a> | PLL_CFG3 | —         | OUT_GATE_TYPE |    | OUT_GATE    | RATIO_CFG | —  |   |            | AUX_OUT_CFG | — | REF_CLK_IN_DIV |   | SYSCLK_SRC |             | —            |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |
| 0x0000 001E<br><a href="#">p. 47</a> | PLL_CFG4 | —         |               |    |             |           |    |   | FLL_BW_MOD | FLL_BW      |   |                | — |            |             |              |              |             |
|                                      |          | 0         | 0             | 0  | 0           | 0         | 0  | 0 | 0          | 0           | 0 | 0              | 0 | 0          | 0           | 0            | 0            |             |



| Address              | Register                    | 15                | 14            | 13           | 12 | 11        | 10           | 9 | 8      | 7                     | 6                   | 5                   | 4                     | 3        | 2                   | 1           | 0             |
|----------------------|-----------------------------|-------------------|---------------|--------------|----|-----------|--------------|---|--------|-----------------------|---------------------|---------------------|-----------------------|----------|---------------------|-------------|---------------|
| 0x0000 0058<br>p. 47 | SW_RESET                    | —                 |               |              |    |           |              |   |        | SW_RST                |                     |                     |                       |          |                     |             |               |
| 0x0000 0064<br>p. 47 | DRIVE_STRENGTH1             | —                 | FSYNC_OUT_DRV |              |    | —         | BCLK_OUT_DRV |   |        | —                     | AUX1_OUT_DRV        |                     |                       | —        | CLK_OUT_DRV         |             |               |
| 0x0000 0100<br>p. 48 | OUTPUT_CFG1                 | BCLK_DIV          |               |              |    | FSYNC_DIV |              |   |        | BCLK_INV              | BCLK_OUT_DIS        | —                   | FSYNC_DUTY_CYCLE      |          |                     | FSYNC_INV   | FSYNC_OUT_DIS |
| 0x0000 0102<br>p. 48 | OUTPUT_CFG2                 | CLK_IN_INV        | —             | AUX1_OUT_SEL |    |           | AUX2_OUT_SEL |   |        | —                     |                     |                     | CLK_OUT_SEL           |          |                     | CLK_OUT_INV | —             |
| 0x0000 0104<br>p. 49 | AUTOMATIC_RATE_CONTROL_CFG1 | —                 |               |              |    |           |              |   |        | ARC_EN                | ARC_BCLK_DIV        |                     |                       |          |                     | ARC_MCLK    |               |
| 0x0000 0108<br>p. 49 | PHASE_ALIGNMENT_CFG1        | PHASE_ALIGNMNT_EN | —             |              |    |           |              |   |        | PHASE_ALIGNMNT_STB_EN | PHASE_ALIGNMNT_MODE | PHASE_ALIGNMNT_TRIG | PHASE_ALIGNMENT_SPEED |          | PHASE_ALIGNMENT_THR |             |               |
| 0x0000 0110<br>p. 50 | DEVICE_ID1                  | DEVID             |               |              |    |           |              |   |        |                       |                     |                     |                       |          |                     |             |               |
| 0x0000 0112<br>p. 50 | DEVICE_ID2                  | —                 |               |              |    |           |              |   | AREVID |                       |                     |                     | MTLREVID              |          |                     |             |               |
| 0x0000 0114<br>p. 50 | UNLOCK_INDICATORS           | —                 |               |              |    |           |              |   |        |                       |                     |                     | P_UNLOCK_STICKY       | P_UNLOCK | F_UNLOCK_STICKY     | F_UNLOCK    |               |
| 0x0000 0116<br>p. 51 | ERROR_STS                   | —                 |               |              |    |           |              |   |        | ERR_STS8              | ERR_STS7            | ERR_STS6            | ERR_STS5              | ERR_STS4 | ERR_STS3            | ERR_STS2    | ERR_STS1      |
| 0x0000 0120<br>p. 51 | OTP_VDD_CTRL                | —                 |               |              |    |           |              |   |        |                       |                     |                     | OTP_VDD_EN            | —        | OTP_LDO_DISCH_EN    | OTP_LDO_EN  |               |

## 6.2 KEYS

| Address              | Register     | 15 ... 8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|--------------|----------|----------|---|---|---|---|---|---|---|
| 0x0000 1104<br>p. 52 | USER_KEY_REG | —        | USER_KEY |   |   |   |   |   |   |   |
|                      |              | 0x00     | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 6.3 OTP\_IF

| Address              | Register    | 15                | 14 | 13 | 12 | 11 | 10 | 9                 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|-------------|-------------------|----|----|----|----|----|-------------------|---|---|---|---|---|---|---|---|---|
| 0x0000 2300<br>p. 52 | OTP_IMG_RD1 | OTP_IMG_RD_BYTE2  |    |    |    |    |    | OTP_IMG_RD_BYTE1  |   |   |   |   |   |   |   |   |   |
| 0x0000 2302<br>p. 52 | OTP_IMG_RD2 | OTP_IMG_RD_BYTE4  |    |    |    |    |    | OTP_IMG_RD_BYTE3  |   |   |   |   |   |   |   |   |   |
| 0x0000 2304<br>p. 52 | OTP_IMG_RD3 | OTP_IMG_RD_BYTE6  |    |    |    |    |    | OTP_IMG_RD_BYTE5  |   |   |   |   |   |   |   |   |   |
| 0x0000 2306<br>p. 53 | OTP_IMG_RD4 | OTP_IMG_RD_BYTE8  |    |    |    |    |    | OTP_IMG_RD_BYTE7  |   |   |   |   |   |   |   |   |   |
| 0x0000 2308<br>p. 53 | OTP_IMG_RD5 | OTP_IMG_RD_BYTE10 |    |    |    |    |    | OTP_IMG_RD_BYTE9  |   |   |   |   |   |   |   |   |   |
| 0x0000 230A<br>p. 53 | OTP_IMG_RD6 | OTP_IMG_RD_BYTE12 |    |    |    |    |    | OTP_IMG_RD_BYTE11 |   |   |   |   |   |   |   |   |   |

| Address              | Register     | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|--------------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| 0x0000 230C<br>p. 53 | OTP_IMG_RD7  | OTP_IMG_RD_BYTE14 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE13 |   |   |   |   |   |   |   |
| 0x0000 230E<br>p. 53 | OTP_IMG_RD8  | OTP_IMG_RD_BYTE16 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE15 |   |   |   |   |   |   |   |
| 0x0000 2310<br>p. 54 | OTP_IMG_RD9  | OTP_IMG_RD_BYTE18 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE17 |   |   |   |   |   |   |   |
| 0x0000 2312<br>p. 54 | OTP_IMG_RD10 | OTP_IMG_RD_BYTE20 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE19 |   |   |   |   |   |   |   |
| 0x0000 2314<br>p. 54 | OTP_IMG_RD11 | OTP_IMG_RD_BYTE22 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE21 |   |   |   |   |   |   |   |
| 0x0000 2316<br>p. 54 | OTP_IMG_RD12 | OTP_IMG_RD_BYTE24 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE23 |   |   |   |   |   |   |   |
| 0x0000 2318<br>p. 54 | OTP_IMG_RD13 | OTP_IMG_RD_BYTE26 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE25 |   |   |   |   |   |   |   |
| 0x0000 231A<br>p. 55 | OTP_IMG_RD14 | OTP_IMG_RD_BYTE28 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE27 |   |   |   |   |   |   |   |
| 0x0000 231C<br>p. 55 | OTP_IMG_RD15 | OTP_IMG_RD_BYTE30 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE29 |   |   |   |   |   |   |   |
| 0x0000 231E<br>p. 55 | OTP_IMG_RD16 | OTP_IMG_RD_BYTE32 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE31 |   |   |   |   |   |   |   |
| 0x0000 2320<br>p. 55 | OTP_IMG_RD17 | OTP_IMG_RD_BYTE34 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE33 |   |   |   |   |   |   |   |
| 0x0000 2322<br>p. 55 | OTP_IMG_RD18 | OTP_IMG_RD_BYTE36 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE35 |   |   |   |   |   |   |   |
| 0x0000 2324<br>p. 56 | OTP_IMG_RD19 | OTP_IMG_RD_BYTE38 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE37 |   |   |   |   |   |   |   |
| 0x0000 2326<br>p. 56 | OTP_IMG_RD20 | OTP_IMG_RD_BYTE40 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE39 |   |   |   |   |   |   |   |
| 0x0000 2328<br>p. 56 | OTP_IMG_RD21 | OTP_IMG_RD_BYTE42 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE41 |   |   |   |   |   |   |   |
| 0x0000 232A<br>p. 56 | OTP_IMG_RD22 | OTP_IMG_RD_BYTE44 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE43 |   |   |   |   |   |   |   |
| 0x0000 232C<br>p. 56 | OTP_IMG_RD23 | OTP_IMG_RD_BYTE46 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE45 |   |   |   |   |   |   |   |
| 0x0000 232E<br>p. 57 | OTP_IMG_RD24 | OTP_IMG_RD_BYTE48 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE47 |   |   |   |   |   |   |   |
| 0x0000 2340<br>p. 57 | OTP_IMG_WR1  | OTP_IMG_WR_BYTE2  |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE1  |   |   |   |   |   |   |   |
| 0x0000 2342<br>p. 57 | OTP_IMG_WR2  | OTP_IMG_WR_BYTE4  |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE3  |   |   |   |   |   |   |   |
| 0x0000 2344<br>p. 57 | OTP_IMG_WR3  | OTP_IMG_WR_BYTE6  |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE5  |   |   |   |   |   |   |   |
| 0x0000 2346<br>p. 57 | OTP_IMG_WR4  | OTP_IMG_WR_BYTE8  |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE7  |   |   |   |   |   |   |   |
| 0x0000 2348<br>p. 58 | OTP_IMG_WR5  | OTP_IMG_WR_BYTE10 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE9  |   |   |   |   |   |   |   |
| 0x0000 234A<br>p. 58 | OTP_IMG_WR6  | OTP_IMG_WR_BYTE12 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE11 |   |   |   |   |   |   |   |
| 0x0000 234C<br>p. 58 | OTP_IMG_WR7  | OTP_IMG_WR_BYTE14 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE13 |   |   |   |   |   |   |   |
| 0x0000 234E<br>p. 58 | OTP_IMG_WR8  | OTP_IMG_WR_BYTE16 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE15 |   |   |   |   |   |   |   |
| 0x0000 2350<br>p. 58 | OTP_IMG_WR9  | OTP_IMG_WR_BYTE18 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE17 |   |   |   |   |   |   |   |

| Address              | Register     | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------------|--------------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| 0x0000 2352<br>p. 59 | OTP_IMG_WR10 | OTP_IMG_WR_BYTE20 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE19 |   |   |   |   |   |   |   |
| 0x0000 2354<br>p. 59 | OTP_IMG_WR11 | OTP_IMG_WR_BYTE22 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE21 |   |   |   |   |   |   |   |
| 0x0000 2356<br>p. 59 | OTP_IMG_WR12 | OTP_IMG_WR_BYTE24 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE23 |   |   |   |   |   |   |   |
| 0x0000 2358<br>p. 59 | OTP_IMG_WR13 | OTP_IMG_WR_BYTE26 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE25 |   |   |   |   |   |   |   |
| 0x0000 235A<br>p. 59 | OTP_IMG_WR14 | OTP_IMG_WR_BYTE28 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE27 |   |   |   |   |   |   |   |
| 0x0000 235C<br>p. 60 | OTP_IMG_WR15 | OTP_IMG_WR_BYTE30 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE29 |   |   |   |   |   |   |   |
| 0x0000 235E<br>p. 60 | OTP_IMG_WR16 | OTP_IMG_WR_BYTE32 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE31 |   |   |   |   |   |   |   |
| 0x0000 2360<br>p. 60 | OTP_IMG_WR17 | OTP_IMG_WR_BYTE34 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE33 |   |   |   |   |   |   |   |
| 0x0000 2362<br>p. 60 | OTP_IMG_WR18 | OTP_IMG_WR_BYTE36 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE35 |   |   |   |   |   |   |   |
| 0x0000 2364<br>p. 60 | OTP_IMG_WR19 | OTP_IMG_WR_BYTE38 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE37 |   |   |   |   |   |   |   |
| 0x0000 2366<br>p. 61 | OTP_IMG_WR20 | OTP_IMG_WR_BYTE40 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE39 |   |   |   |   |   |   |   |
| 0x0000 2368<br>p. 61 | OTP_IMG_WR21 | OTP_IMG_WR_BYTE42 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE41 |   |   |   |   |   |   |   |
| 0x0000 236A<br>p. 61 | OTP_IMG_WR22 | OTP_IMG_WR_BYTE44 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE43 |   |   |   |   |   |   |   |
| 0x0000 236C<br>p. 61 | OTP_IMG_WR23 | OTP_IMG_WR_BYTE46 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE45 |   |   |   |   |   |   |   |
| 0x0000 236E<br>p. 61 | OTP_IMG_WR24 | OTP_IMG_WR_BYTE48 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE47 |   |   |   |   |   |   |   |

## 6.4 OTP\_CTRL

| Address              | Register  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0           |   |
|----------------------|-----------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------------|---|
| 0x0000 2400<br>p. 62 | OTP_CTRL1 | —  |    |    |    |    |    |   |   |   |   |   |   |   |   |   | OTP_PROG_EN | — |
|                      |           | 0  | 0  | 0  | 0  | 0  | 1  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0           |   |

## 6.5 OTP\_STS

| Address              | Register | 15 | 14 | 13 | 12 | 11         | 10 | 9 | 8               | 7 | 6           | 5 | 4 | 3 | 2 | 1 | 0        |  |
|----------------------|----------|----|----|----|----|------------|----|---|-----------------|---|-------------|---|---|---|---|---|----------|--|
| 0x0000 24A8<br>p. 62 | OTP_STS2 | —  |    |    |    | OTP_IMG_ID |    |   |                 | — |             |   |   |   |   |   |          |  |
|                      |          | 0  | 0  | 0  | 0  | 0          | 0  | 0 | 0               | 0 | 0           | 0 | 0 | 0 | 0 | 0 | 0        |  |
| 0x0000 24AC<br>p. 62 | OTP_STS3 | —  |    |    |    |            |    |   | OTP_IMG_ECC_STS |   | —           |   |   |   |   |   |          |  |
|                      |          | 0  | 0  | 0  | 0  | 0          | 0  | 0 | 0               | 0 | 0           | 0 | 0 | 0 | 0 | 0 | 0        |  |
| 0x0000 24BC<br>p. 62 | OTP_STS6 | —  |    |    |    |            |    |   |                 |   | OTP_IMG_NUM |   |   | — |   |   | OTP_MODE |  |
|                      |          | 0  | 0  | 0  | 0  | 0          | 0  | 0 | 0               | 0 | 0           | 0 | 0 | 0 | 0 | 0 | 0        |  |

## 7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS2600.

- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- Fields shown in orange are affected by the FREEZE bit.
- All visible fields are read/write except where indicated with the following shading:

Read/write access     
  Read-only access     
  Write-only access     
  User key password access

### 7.1 CONFIG

#### 7.1.1 PLL\_CFG1

Address: 0x0000 0002

|         |           |    |    |             |    |    |   |         |   |   |   |   |              |             |   |   |
|---------|-----------|----|----|-------------|----|----|---|---------|---|---|---|---|--------------|-------------|---|---|
| RW      | 15        | 14 | 13 | 12          | 11 | 10 | 9 | 8       | 7 | 6 | 5 | 4 | 3            | 2           | 1 | 0 |
|         | RATIO_MOD |    |    | S_RATIO_SEL |    | —  |   | PLL_EN1 | — |   |   |   | AUX1_OUT_DIS | CLK_OUT_DIS |   |   |
| Default | 0         | 0  | 0  | 0           | 0  | 0  | 0 | 0       | 1 | 0 | 0 | 0 | 0            | 0           | 0 | 0 |

| Bits  | Name         | Description  |
|-------|--------------|--|
| 15:13 | RATIO_MOD    | Ratio modifier control. Adjusts the PLL ratio by the selected multiplier/division factor.<br>000 = (Default) Multiply x1      100 = Divide /2<br>001 = Multiply x2      101 = Divide /4<br>010 = Multiply x4      110 = Divide /8<br>011 = Multiply x8      111 = Divide /16 |
| 12:11 | S_RATIO_SEL  | Ratio selection in Synthesizer Mode.<br>00 = (Default) Ratio 1      10 = Ratio 3<br>01 = Ratio 2      11 = Ratio 4   |
| 10:9  | —            | Reserved   |
| 8     | PLL_EN1      | PLL enable. Note that PLL_EN2 must also be set to enable the PLL.<br>0 = (Default) Disabled<br>1 = Enabled   |
| 7:2   | —            | Reserved   |
| 1     | AUX1_OUT_DIS | AUX1_OUT disable. If disabled, the output driver is high-impedance (Hi-Z).<br>0 = (Default) Output enabled<br>1 = Output disabled (Hi-Z)   |
| 0     | CLK_OUT_DIS  | CLK_OUT disable. If disabled, the output driver is high-impedance (Hi-Z).<br>0 = (Default) Output enabled<br>1 = Output disabled (Hi-Z)  |

#### 7.1.2 PLL\_CFG2

Address: 0x0000 0004

|         |    |    |    |    |           |    |   |         |   |   |   |   |             |              |   |   |
|---------|----|----|----|----|-----------|----|---|---------|---|---|---|---|-------------|--------------|---|---|
| RW      | 15 | 14 | 13 | 12 | 11        | 10 | 9 | 8       | 7 | 6 | 5 | 4 | 3           | 2            | 1 | 0 |
|         | —  |    |    |    | FREEZE_EN | —  |   | PLL_EN2 | — |   |   |   | M_RATIO_SEL | PLL_MODE_SEL |   |   |
| Default | 0  | 0  | 0  | 0  | 0         | 0  | 0 | 0       | 0 | 0 | 0 | 0 | 1           | 0            | 0 | 0 |

| Bits  | Name      | Description  |
|-------|-----------|--|
| 15:12 | —         | Reserved   |
| 11    | FREEZE_EN | Freeze register control. If enabled, the freezable fields hold their current values. Any updates to these fields are buffered until FREEZE_EN is cleared.<br>0 = (Default) Disabled<br>1 = Enabled |
| 10:9  | —         | Reserved   |

| Bits | Name         | Description  |
|------|--------------|--|
| 8    | PLL_EN2      | PLL enable. Note that PLL_EN1 must also be set to enable the PLL.<br>0 = (Default) Disabled<br>1 = Enabled   |
| 7:3  | —            | Reserved   |
| 2:1  | M_RATIO_SEL  | Ratio selection in Multiplier Mode.<br>00 = (Default) Ratio 1<br>01 = Ratio 2<br>10 = Ratio 3<br>11 = Ratio 4  |
| 0    | PLL_MODE_SEL | PLL mode control. Selects Multiplier Mode or Synthesizer Mode. Only valid if S_RATIO_SEL and M_RATIO_SEL are set to the same value.<br>0 = (Default) Synthesizer Mode<br>1 = Multiplier Mode |

**7.1.3 RATIO1\_1**
**Address: 0x0000 0006**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO1_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description            |
|------|----------|------------------------|
| 15:0 | RATIO1_1 | Ratio 1, bits [31:16]. |

**7.1.4 RATIO1\_2**
**Address: 0x0000 0008**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO1_2 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description           |
|------|----------|-----------------------|
| 15:0 | RATIO1_2 | Ratio 1, bits [15:0]. |

**7.1.5 RATIO2\_1**
**Address: 0x0000 000A**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO2_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description            |
|------|----------|------------------------|
| 15:0 | RATIO2_1 | Ratio 2, bits [31:16]. |

**7.1.6 RATIO2\_2**
**Address: 0x0000 000C**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO2_2 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description           |
|------|----------|-----------------------|
| 15:0 | RATIO2_2 | Ratio 2, bits [15:0]. |

**7.1.7 RATIO3\_1**
**Address: 0x0000 000E**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO3_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description            |
|------|----------|------------------------|
| 15:0 | RATIO3_1 | Ratio 3, bits [31:16]. |

**7.1.8 RATIO3\_2**
**Address: 0x0000 0010**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO3_2 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description           |
|------|----------|-----------------------|
| 15:0 | RATIO3_2 | Ratio 3, bits [15:0]. |

**7.1.9 RATIO4\_1**
**Address: 0x0000 0012**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO4_1 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description            |
|------|----------|------------------------|
| 15:0 | RATIO4_1 | Ratio 4, bits [31:16]. |

**7.1.10 RATIO4\_2**
**Address: 0x0000 0014**

|         |          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|----------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RW      | 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | RATIO4_2 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0        | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description           |
|------|----------|-----------------------|
| 15:0 | RATIO4_2 | Ratio 4, bits [15:0]. |

**7.1.11 PLL\_CFG3**
**Address: 0x0000 0016**

|         |    |               |          |           |    |    |   |   |             |   |   |                |            |   |   |   |
|---------|----|---------------|----------|-----------|----|----|---|---|-------------|---|---|----------------|------------|---|---|---|
| RW      | 15 | 14            | 13       | 12        | 11 | 10 | 9 | 8 | 7           | 6 | 5 | 4              | 3          | 2 | 1 | 0 |
|         | —  | OUT_GATE_TYPE | OUT_GATE | RATIO_CFG | —  | —  | — | — | AUX_OUT_CFG | — | — | REF_CLK_IN_DIV | SYSCLK_SRC | — | — | — |
| Default | 0  | 0             | 0        | 0         | 0  | 0  | 0 | 0 | 0           | 0 | 0 | 0              | 0          | 0 | 0 | 0 |

| Bits  | Name           | Description  |
|-------|----------------|--|
| 15    | —              | Reserved   |
| 14:13 | OUT_GATE_TYPE  | Output gate type. Selects the logic condition used to determine if the outputs are valid.<br>00 = (Default) Frequency unlock (F_UNLOCK)      10 = Analog PLL unlock<br>01 = Phase unlock (P_UNLOCK)                      11 = Reserved   |
| 12    | OUT_GATE       | Output gate control. Selects whether the clock outputs are stopped automatically if they are not valid.<br>0 = (Default) Enabled<br>1 = Disabled   |
| 11    | RATIO_CFG      | Ratio format control. Selects format for the ratio selected by M_RATIO_SEL. Note this field has no effect in Synthesizer Mode.<br>0 = (Default) High multiplication (20.12)<br>1 = High resolution (12.20)   |
| 10:7  | —              | Reserved   |
| 6     | AUX_OUT_CFG    | AUX1 and AUX2 driver configuration. Only valid for lock/status output signals; clock outputs are CMOS in all cases.<br>0 = (Default) CMOS. Active high (Logic 1 indicates unlock or clock-missing status).<br>1 = Open Drain. Active low (Logic 0 indicates unlock or clock-missing status). |
| 5     | —              | Reserved   |
| 4:3   | REF_CLK_IN_DIV | REF_CLK_IN input divider.<br>00 = (Default) Divide by 4                              10 = Divide by 1<br>01 = Divide by 2                                        11 = Reserved   |
| 2:1   | SYSCLK_SRC     | Source selection for the PLL timing reference SYSCLK between REF_CLK_IN and the internal oscillator<br>00 = (Default) Automatic selection              10 = Internal oscillator<br>01 = REF_CLK_IN                                      11 = Reserved  |
| 0     | —              | Reserved   |

**7.1.12 PLL\_CFG4**
**Address: 0x0000 001E**

|         |        |            |        |   |   |   |   |   |   |
|---------|--------|------------|--------|---|---|---|---|---|---|
| RW      | 15...8 | 7          | 6      | 5 | 4 | 3 | 2 | 1 | 0 |
|         | —      | FLL_BW_MOD | FLL_BW |   |   | — |   |   |   |
| Default | 0x00   | 0          | 0      | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name       | Description  |
|------|------------|--|
| 15:8 | —          | Reserved   |
| 7    | FLL_BW_MOD | FLL bandwidth multiplication factor. Modifies the bandwidth selected by FLL_BW.<br>0 = (Default) FLL_BW is multiplied by 1<br>1 = FLL_BW is multiplied by 16                         |
| 6:4  | FLL_BW     | FLL bandwidth select. Note the FLL bandwidth is also determined by the multiplication factor, FLL_BW_MOD.<br>000 = (Default) 1 Hz<br>001 = 2 Hz<br>010 = 4 Hz<br>...<br>111 = 128 Hz |
| 3:0  | —          | Reserved   |

**7.1.13 SW\_RESET**
**Address: 0x0000 0058**

|         |        |        |   |   |   |   |   |   |   |
|---------|--------|--------|---|---|---|---|---|---|---|
| WO      | 15...8 | 7      | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | —      | SW_RST |   |   |   |   |   |   |   |
| Default | 0x00   | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name   | Description  |
|------|--------|--|
| 15:8 | —      | Reserved   |
| 7:0  | SW_RST | Software reset. Write 0x5A to execute a software reset.<br>0x00 = (Default) No action<br>0x01–0x59 = Reserved<br>0x5A = Software reset<br>0x5B–0xFF = Reserved |

**7.1.14 DRIVE\_STRENGTH1**
**Address: 0x0000 0064**

|         |    |               |    |    |    |    |              |   |   |   |              |   |   |   |             |   |
|---------|----|---------------|----|----|----|----|--------------|---|---|---|--------------|---|---|---|-------------|---|
| RW      | 15 | 14            | 13 | 12 | 11 | 10 | 9            | 8 | 7 | 6 | 5            | 4 | 3 | 2 | 1           | 0 |
|         | —  | FSYNC_OUT_DRV |    |    |    | —  | BCLK_OUT_DRV |   |   | — | AUX1_OUT_DRV |   |   | — | CLK_OUT_DRV |   |
| Default | 0  | 1             | 0  | 0  | 0  | 1  | 0            | 0 | 0 | 1 | 0            | 0 | 0 | 1 | 0           | 0 |

| Bits  | Name          | Description   |
|-------|---------------|---|
| 15    | —             | Reserved  |
| 14:12 | FSYNC_OUT_DRV | FSYNC_OUT drive strength.<br>000 = 2 mA<br>001 = 4 mA<br>...<br>100 = (Default) 10 mA<br>...<br>111 = 16 mA |
| 11    | —             | Reserved  |
| 10:8  | BCLK_OUT_DRV  | BCLK_OUT drive strength.<br>000 = 2 mA<br>001 = 4 mA<br>...<br>100 = (Default) 10 mA<br>...<br>111 = 16 mA  |
| 7     | —             | Reserved  |
| 6:4   | AUX1_OUT_DRV  | AUX1_OUT drive strength.<br>000 = 2 mA<br>001 = 4 mA<br>...<br>100 = (Default) 10 mA<br>...<br>111 = 16 mA  |
| 3     | —             | Reserved  |
| 2:0   | CLK_OUT_DRV   | CLK_OUT drive strength.<br>000 = 2 mA<br>001 = 4 mA<br>...<br>100 = (Default) 10 mA<br>...<br>111 = 16 mA   |

**7.1.15 OUTPUT\_CFG1**
**Address: 0x0000 0100**

|         |          |    |    |    |           |    |   |   |          |              |   |                  |   |   |           |               |
|---------|----------|----|----|----|-----------|----|---|---|----------|--------------|---|------------------|---|---|-----------|---------------|
| RW      | 15       | 14 | 13 | 12 | 11        | 10 | 9 | 8 | 7        | 6            | 5 | 4                | 3 | 2 | 1         | 0             |
|         | BCLK_DIV |    |    |    | FSYNC_DIV |    |   |   | BCLK_INV | BCLK_OUT_DIS | — | FSYNC_DUTY_CYCLE |   |   | FSYNC_INV | FSYNC_OUT_DIS |
| Default | 0        | 0  | 0  | 0  | 0         | 0  | 0 | 0 | 0        | 0            | 0 | 0                | 0 | 0 | 0         | 0             |

| Bits  | Name             | Description  |
|-------|------------------|--|
| 15:12 | BCLK_DIV         | BCLK output divider. Note this field has no effect if automatic rate control (ARC) is enabled.<br>0x0 = (Default) Divide by 1<br>0x1 = Divide by 2<br>0x2 = Divide by 3<br>0x3 = Divide by 4<br>0x4 = Divide by 6<br>0x5 = Divide by 8<br>0x6 = Divide by 12<br>0x7 = Divide by 16<br>0x8 = Divide by 24<br>0x9 = Divide by 32<br>0xA = Divide by 48<br>0xB–0xF = Reserved   |
| 11:8  | FSYNC_DIV        | FSYNC output divider. Note this field has no effect if automatic rate control (ARC) is enabled.<br>0x0 = (Default) Divide by 16<br>0x1 = Divide by 32<br>0x2 = Divide by 64<br>0x3 = Divide by 128<br>0x4 = Divide by 256<br>0x5 = Divide by 512<br>0x6 = Divide by 1024<br>0x7 = Divide by 192<br>0x8 = Divide by 384<br>0x9 = Divide by 768<br>0xA = Divide by 1536<br>0xB = Divide by 576<br>0xC = Divide by 1152<br>0xD–0xF = Reserved |
| 7     | BCLK_INV         | BCLK polarity select.<br>0 = (Default) Normal<br>1 = Inverted  |
| 6     | BCLK_OUT_DIS     | BCLK_OUT disable. If disabled, the output driver is high-impedance (Hi-Z).<br>0 = (Default) Output enabled<br>1 = Output disabled (Hi-Z)   |
| 5     | —                | Reserved   |
| 4:2   | FSYNC_DUTY_CYCLE | FSYNC output duty-cycle control. Note the FSYNC duty cycle must be configured less than or equal to 50%.<br>000 = (Default) 50% duty cycle<br>001 = 1 BCLK period<br>010 = 2 BCLK periods<br>011 = 4 BCLK periods<br>100 = 8 BCLK periods<br>101 = 16 BCLK periods<br>110 = 32 BCLK periods<br>111 = Reserved  |
| 1     | FSYNC_INV        | FSYNC polarity select.<br>0 = (Default) Normal<br>1 = Inverted   |
| 0     | FSYNC_OUT_DIS    | FSYNC_OUT disable. If disabled, the output driver is high-impedance (Hi-Z).<br>0 = (Default) Output enabled<br>1 = Output disabled (Hi-Z)  |

**7.1.16 OUTPUT\_CFG2**
**Address: 0x0000 0102**

|         |            |    |              |    |    |              |   |   |   |   |             |   |             |   |   |   |
|---------|------------|----|--------------|----|----|--------------|---|---|---|---|-------------|---|-------------|---|---|---|
| RW      | 15         | 14 | 13           | 12 | 11 | 10           | 9 | 8 | 7 | 6 | 5           | 4 | 3           | 2 | 1 | 0 |
|         | CLK_IN_INV | —  | AUX1_OUT_SEL |    |    | AUX2_OUT_SEL |   | — |   |   | CLK_OUT_SEL |   | CLK_OUT_INV | — |   |   |
| Default | 0          | 0  | 0            | 0  | 0  | 0            | 0 | 0 | 0 | 0 | 0           | 0 | 0           | 0 | 0 | 0 |

| Bits  | Name         | Description   |
|-------|--------------|---|
| 15    | CLK_IN_INV   | CLK_IN polarity select.<br>0 = (Default) Normal<br>1 = Inverted   |
| 14:13 | —            | Reserved  |
| 12:10 | AUX1_OUT_SEL | AUX1_OUT function select.<br>000 = (Default) REF_CLK_IN<br>001 = CLK_IN<br>010 = CLK_OUT<br>011 = Frequency unlock (F_UNLOCK)<br>100 = Phase unlock (P_UNLOCK)<br>101 = BCLK<br>110 = FSYNC<br>111 = CLK_IN (clock missing) |
| 9:8   | AUX2_OUT_SEL | AUX2_OUT function select.<br>00 = (Default) Disabled<br>01 = Frequency unlock (F_UNLOCK)<br>10 = Phase unlock (P_UNLOCK)<br>11 = CLK_IN (clock missing)   |
| 7:4   | —            | Reserved  |



| Bits | Name        | Description   |
|------|-------------|---|
| 3:2  | CLK_OUT_SEL | CLK_OUT function. Selects clock source for CLK_OUT.<br>00 = (Default) MCLK<br>01 = ALTCLK 352.8/384.0 kHz<br>10 = ALTCLK 1.882/2.048 MHz<br>11 = ALTCLK 2.053/2.234 MHz |
| 1    | CLK_OUT_INV | CLK_OUT polarity select.<br>0 = (Default) Normal<br>1 = Inverted  |
| 0    | —           | Reserved  |

**7.1.17 AUTOMATIC\_RATE\_CONTROL\_CFG1**
**Address: 0x0000 0104**

|         |        |   |        |              |   |   |          |   |   |
|---------|--------|---|--------|--------------|---|---|----------|---|---|
| RW      | 15...8 | 7 | 6      | 5            | 4 | 3 | 2        | 1 | 0 |
|         | —      | — | ARC_EN | ARC_BCLK_DIV |   |   | ARC_MCLK |   |   |
| Default | 0x00   | 0 | 0      | 0            | 0 | 0 | 0        | 0 | 0 |

| Bits | Name         | Description  |
|------|--------------|--|
| 15:7 | —            | Reserved   |
| 6    | ARC_EN       | Automatic rate control (ARC) enable.<br>0 = (Default) Disabled<br>1 = Enabled  |
| 5:2  | ARC_BCLK_DIV | BCLK output control in ARC mode.<br>0x0 = (Default) FSYNC x64<br>0x1 = FSYNC x128<br>0x2 = FSYNC x256<br>0x3 = FSYNC x512<br>0x4 = FSYNC x1024<br>0x5 = MCLK /1<br>0x6 = MCLK /2<br>0x7 = MCLK /4<br>0x8 = MCLK /8<br>0x9 = MCLK /16<br>0xA–0xF = Reserved |
| 1:0  | ARC_MCLK     | MCLK output control in ARC mode. Note the output frequency depends on whether the clock reference is a multiple of 48 kHz or 44.1 kHz.<br>00 = (Default) 12.288/11.2896 MHz<br>01 = 24.576/22.5792 MHz<br>10 = 49.152/45.1584 MHz<br>11 = Reserved         |

**7.1.18 PHASE\_ALIGNMENT\_CFG1**
**Address: 0x0000 0108**

|         |                    |    |    |    |    |    |   |                        |                      |                      |                       |   |   |                     |   |   |
|---------|--------------------|----|----|----|----|----|---|------------------------|----------------------|----------------------|-----------------------|---|---|---------------------|---|---|
|         | 15                 | 14 | 13 | 12 | 11 | 10 | 9 | 8                      | 7                    | 6                    | 5                     | 4 | 3 | 2                   | 1 | 0 |
|         | PHASE_ALIGNMENT_EN | —  |    |    |    |    |   | PHASE_ALIGNMENT_STB_EN | PHASE_ALIGNMENT_MODE | PHASE_ALIGNMENT_TRIG | PHASE_ALIGNMENT_SPEED |   |   | PHASE_ALIGNMENT_THR |   |   |
| Access  | RW                 | —  |    |    |    |    |   | RW                     | RW                   | WO                   | RW                    |   |   | RW                  |   |   |
| Default | 0                  | 0  | 0  | 0  | 0  | 0  | 0 | 0                      | 0                    | 0                    | 0                     | 0 | 0 | 0                   | 0 | 0 |

| Bits | Name                   | Description   |
|------|------------------------|---|
| 15   | PHASE_ALIGNMENT_EN     | Phase-alignment enable.<br>0 = (Default) Disabled<br>1 = Enabled  |
| 14:8 | —                      | Reserved  |
| 7    | PHASE_ALIGNMENT_STB_EN | Phase-alignment stability control. If this bit is set, the phase-alignment process is only executed if the phase offset is stable.<br>0 = (Default) Disabled<br>1 = Enabled |
| 6    | PHASE_ALIGNMENT_MODE   | Phase-alignment trigger mode.<br>0 = (Default) Automatic<br>1 = Manual  |
| 5    | PHASE_ALIGNMENT_TRIG   | Phase-alignment manual trigger. Write 1 to trigger the phase-alignment process in manual mode.<br>0 = (Default) No action<br>1 = Trigger                                    |

| Bits | Name                  | Description  |
|------|-----------------------|--|
| 4:3  | PHASE_ALIGNMENT_SPEED | Phase-alignment speed. Selects the phase-alignment rate by configuring the maximum permitted stretching of the FSYNC cycle.<br>00 = (Default) 1 MCLK per FSYNC cycle<br>01 = 10 MCLK per FSYNC cycle<br>10 = 50 MCLK per FSYNC cycle<br>11 = Maximum   |
| 2:0  | PHASE_ALIGNMENT_THR   | Phase-alignment threshold. Selects the phase-offset threshold to trigger the phase-alignment process in automatic mode.<br>000 = (Default) 2 MCLK periods<br>001 = 4 MCLK periods<br>010 = 8 MCLK periods<br>011 = 16 MCLK periods<br>100 = 32 MCLK periods<br>101 = 64 MCLK periods<br>110 = 128 MCLK periods<br>111 = 256 MCLK periods |

**7.1.19 DEVICE\_ID1**
**Address: 0x0000 0110**

|         |       |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---------|-------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| RO      | 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | DEVID |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| Default | 0     | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name  | Description  |
|------|-------|--|
| 15:0 | DEVID | Device ID. A value of 0x2600 indicates the device is a CS2600. |

**7.1.20 DEVICE\_ID2**
**Address: 0x0000 0112**

|         |        |   |   |   |          |   |   |   |   |
|---------|--------|---|---|---|----------|---|---|---|---|
| RO      | 15...8 | 7 | 6 | 5 | 4        | 3 | 2 | 1 | 0 |
|         | AREVID |   |   |   | MTLREVID |   |   |   |   |
| Default | 0x00   | X | X | X | X        | X | X | X | X |

| Bits | Name     | Description  |
|------|----------|--|
| 15:8 | —        | Reserved   |
| 7:4  | AREVID   | All-layer device revision. This field is incremented for every all-layer revision of the device.     |
| 3:0  | MTLREVID | Metal-layer device revision. This field is incremented for every metal-layer revision of the device. |

**7.1.21 UNLOCK\_INDICATORS**
**Address: 0x0000 0114**

|         |        |   |   |   |                 |   |          |   |                 |  |          |
|---------|--------|---|---|---|-----------------|---|----------|---|-----------------|--|----------|
|         | 15...8 | 7 | 6 | 5 | 4               | 3 | 2        | 1 | 0               |  |          |
|         |        |   |   |   | P_UNLOCK_STICKY |   | P_UNLOCK |   | F_UNLOCK_STICKY |  | F_UNLOCK |
| Access  |        |   |   |   | W1C             |   | RO       |   | W1C             |  | RO       |
| Default | 0x00   | 0 | 0 | 0 | 0               | 0 | X        | 0 | X               |  |          |

| Bits | Name            | Description  |
|------|-----------------|--|
| 15:4 | —               | Reserved   |
| 3    | P_UNLOCK_STICKY | Phase-unlock status. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Locked<br>1 = Unlocked     |
| 2    | P_UNLOCK        | Phase-unlock status.<br>0 = Locked<br>1 = Unlocked   |
| 1    | F_UNLOCK_STICKY | Frequency-unlock status. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Locked<br>1 = Unlocked |
| 0    | F_UNLOCK        | Frequency-unlock status.<br>0 = Locked<br>1 = Unlocked   |

**7.1.22 ERROR\_STS**
**Address: 0x0000 0116**

|         |        |          |          |          |          |          |          |          |          |
|---------|--------|----------|----------|----------|----------|----------|----------|----------|----------|
| W1C     | 15...8 | 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|         | —      | ERR_STS8 | ERR_STS7 | ERR_STS6 | ERR_STS5 | ERR_STS4 | ERR_STS3 | ERR_STS2 | ERR_STS1 |
| Default | 0x00   | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

| Bits | Name     | Description   |
|------|----------|---|
| 15:8 | —        | Reserved  |
| 7    | ERR_STS8 | Error status bit indicates the device is defective. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error        |
| 6    | ERR_STS7 | Error status bit indicates the OTP memory is corrupt. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error      |
| 5    | ERR_STS6 | Error status bit indicates invalid register configuration. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error |
| 4    | ERR_STS5 | Error status bit indicates the PLL is disabled. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error            |
| 3    | ERR_STS4 | Error status bit indicates invalid hardware configuration. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error |
| 2    | ERR_STS3 | Error status bit indicates REF_CLK_IN is not present. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error      |
| 1    | ERR_STS2 | Error status bit indicates CLK_IN is not stable. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error           |
| 0    | ERR_STS1 | Error status bit indicates CLK_IN is not present. This bit is latching when set, it remains set until cleared by writing 1.<br>0 = (Default) Normal<br>1 = Error          |

**7.1.23 OTP\_VDD\_CTRL**
**Address: 0x0000 0120**

|         |        |   |   |   |   |            |   |                  |            |
|---------|--------|---|---|---|---|------------|---|------------------|------------|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3          | 2 | 1                | 0          |
|         | —      | — | — | — | — | OTP_VDD_EN | — | OTP_LDO_DISCH_EN | OTP_LDO_EN |
| Default | 0x00   | 0 | 0 | 0 | 0 | 0          | 0 | 0                | 0          |

| Bits | Name             | Description   |
|------|------------------|---|
| 15:4 | —                | Reserved  |
| 3    | OTP_VDD_EN       | Enables the OTP programming supply<br>0 = (Default) Disabled<br>1 = Enabled |
| 2    | —                | Reserved  |
| 1    | OTP_LDO_DISCH_EN | LDO output discharge<br>0 = (Default) Disabled<br>1 = Enabled               |
| 0    | OTP_LDO_EN       | LDO enable (for OTP programming)<br>0 = (Default) Disabled<br>1 = Enabled   |

## 7.2 KEYS

### 7.2.1 USER\_KEY\_REG

**Address: 0x0000 1104**

|         |        |          |   |   |   |   |   |   |   |
|---------|--------|----------|---|---|---|---|---|---|---|
| WO      | 15...8 | 7        | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | —      | USER_KEY |   |   |   |   |   |   |   |
| Default | 0x00   | 0        | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name     | Description   |
|------|----------|---|
| 15:8 | —        | Reserved  |
| 7:0  | USER_KEY | User Key control – requires two writes to set (unlock):<br>0xAA followed by 0x55 sets the key<br>A write of any other byte value unsets (locks) the key |

## 7.3 OTP\_IF

### 7.3.1 OTP\_IMG\_RD1

**Address: 0x0000 2300**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE2 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE1 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                 |
|------|------------------|-----------------------------|
| 15:8 | OTP_IMG_RD_BYTE2 | OTP image byte 2 read field |
| 7:0  | OTP_IMG_RD_BYTE1 | OTP image byte 1 read field |

### 7.3.2 OTP\_IMG\_RD2

**Address: 0x0000 2302**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE4 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE3 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                 |
|------|------------------|-----------------------------|
| 15:8 | OTP_IMG_RD_BYTE4 | OTP image byte 4 read field |
| 7:0  | OTP_IMG_RD_BYTE3 | OTP image byte 3 read field |

### 7.3.3 OTP\_IMG\_RD3

**Address: 0x0000 2304**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE6 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE5 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                 |
|------|------------------|-----------------------------|
| 15:8 | OTP_IMG_RD_BYTE6 | OTP image byte 6 read field |
| 7:0  | OTP_IMG_RD_BYTE5 | OTP image byte 5 read field |

**7.3.4 OTP\_IMG\_RD4**
**Address: 0x0000 2306**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE8 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE7 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                 |
|------|------------------|-----------------------------|
| 15:8 | OTP_IMG_RD_BYTE8 | OTP image byte 8 read field |
| 7:0  | OTP_IMG_RD_BYTE7 | OTP image byte 7 read field |

**7.3.5 OTP\_IMG\_RD5**
**Address: 0x0000 2308**

|         |                   |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE10 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE9 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE10 | OTP image byte 10 read field |
| 7:0  | OTP_IMG_RD_BYTE9  | OTP image byte 9 read field  |

**7.3.6 OTP\_IMG\_RD6**
**Address: 0x0000 230A**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE12 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE11 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE12 | OTP image byte 12 read field |
| 7:0  | OTP_IMG_RD_BYTE11 | OTP image byte 11 read field |

**7.3.7 OTP\_IMG\_RD7**
**Address: 0x0000 230C**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE14 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE13 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE14 | OTP image byte 14 read field |
| 7:0  | OTP_IMG_RD_BYTE13 | OTP image byte 14 read field |

**7.3.8 OTP\_IMG\_RD8**
**Address: 0x0000 230E**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE16 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE15 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE16 | OTP image byte 16 read field |
| 7:0  | OTP_IMG_RD_BYTE15 | OTP image byte 15 read field |

**7.3.9 OTP\_IMG\_RD9**
**Address: 0x0000 2310**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE18 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE17 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE18 | OTP image byte 18 read field |
| 7:0  | OTP_IMG_RD_BYTE17 | OTP image byte 17 read field |

**7.3.10 OTP\_IMG\_RD10**
**Address: 0x0000 2312**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE20 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE19 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE20 | OTP image byte 20 read field |
| 7:0  | OTP_IMG_RD_BYTE19 | OTP image byte 19 read field |

**7.3.11 OTP\_IMG\_RD11**
**Address: 0x0000 2314**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE22 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE21 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE22 | OTP image byte 22 read field |
| 7:0  | OTP_IMG_RD_BYTE21 | OTP image byte 21 read field |

**7.3.12 OTP\_IMG\_RD12**
**Address: 0x0000 2316**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE24 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE23 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE24 | OTP image byte 24 read field |
| 7:0  | OTP_IMG_RD_BYTE23 | OTP image byte 23 read field |

**7.3.13 OTP\_IMG\_RD13**
**Address: 0x0000 2318**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE26 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE25 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE26 | OTP image byte 26 read field |
| 7:0  | OTP_IMG_RD_BYTE25 | OTP image byte 25 read field |

**7.3.14 OTP\_IMG\_RD14**
**Address: 0x0000 231A**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE28 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE27 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE28 | OTP image byte 28 read field |
| 7:0  | OTP_IMG_RD_BYTE27 | OTP image byte 27 read field |

**7.3.15 OTP\_IMG\_RD15**
**Address: 0x0000 231C**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE30 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE29 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE30 | OTP image byte 30 read field |
| 7:0  | OTP_IMG_RD_BYTE29 | OTP image byte 29 read field |

**7.3.16 OTP\_IMG\_RD16**
**Address: 0x0000 231E**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE32 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE31 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE32 | OTP image byte 32 read field |
| 7:0  | OTP_IMG_RD_BYTE31 | OTP image byte 31 read field |

**7.3.17 OTP\_IMG\_RD17**
**Address: 0x0000 2320**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE34 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE33 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE34 | OTP image byte 34 read field |
| 7:0  | OTP_IMG_RD_BYTE33 | OTP image byte 33 read field |

**7.3.18 OTP\_IMG\_RD18**
**Address: 0x0000 2322**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE36 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE35 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE36 | OTP image byte 36 read field |
| 7:0  | OTP_IMG_RD_BYTE35 | OTP image byte 35 read field |

**7.3.19 OTP\_IMG\_RD19**
**Address: 0x0000 2324**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE38 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE37 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE38 | OTP image byte 38 read field |
| 7:0  | OTP_IMG_RD_BYTE37 | OTP image byte 37 read field |

**7.3.20 OTP\_IMG\_RD20**
**Address: 0x0000 2326**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE40 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE39 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE40 | OTP image byte 40 read field |
| 7:0  | OTP_IMG_RD_BYTE39 | OTP image byte 39 read field |

**7.3.21 OTP\_IMG\_RD21**
**Address: 0x0000 2328**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE42 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE41 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE42 | OTP image byte 42 read field |
| 7:0  | OTP_IMG_RD_BYTE41 | OTP image byte 41 read field |

**7.3.22 OTP\_IMG\_RD22**
**Address: 0x0000 232A**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE44 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE43 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE44 | OTP image byte 44 read field |
| 7:0  | OTP_IMG_RD_BYTE43 | OTP image byte 43 read field |

**7.3.23 OTP\_IMG\_RD23**
**Address: 0x0000 232C**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE46 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE45 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE46 | OTP image byte 46 read field |
| 7:0  | OTP_IMG_RD_BYTE45 | OTP image byte 45 read field |



**7.3.24 OTP\_IMG\_RD24**
**Address: 0x0000 232E**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_RD_BYTE48 |    |    |    |    |    |   |   | OTP_IMG_RD_BYTE47 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                  |
|------|-------------------|------------------------------|
| 15:8 | OTP_IMG_RD_BYTE48 | OTP image byte 48 read field |
| 7:0  | OTP_IMG_RD_BYTE47 | OTP image byte 47 read field |

**7.3.25 OTP\_IMG\_WR1**
**Address: 0x0000 2340**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE2 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE1 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                  |
|------|------------------|------------------------------|
| 15:8 | OTP_IMG_WR_BYTE2 | OTP image byte 2 write field |
| 7:0  | OTP_IMG_WR_BYTE1 | OTP image byte 1 write field |

**7.3.26 OTP\_IMG\_WR2**
**Address: 0x0000 2342**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE4 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE3 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                  |
|------|------------------|------------------------------|
| 15:8 | OTP_IMG_WR_BYTE4 | OTP image byte 4 write field |
| 7:0  | OTP_IMG_WR_BYTE3 | OTP image byte 3 write field |

**7.3.27 OTP\_IMG\_WR3**
**Address: 0x0000 2344**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE6 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE5 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                  |
|------|------------------|------------------------------|
| 15:8 | OTP_IMG_WR_BYTE6 | OTP image byte 6 write field |
| 7:0  | OTP_IMG_WR_BYTE5 | OTP image byte 5 write field |

**7.3.28 OTP\_IMG\_WR4**
**Address: 0x0000 2346**

|         |                  |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE8 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE7 |   |   |   |   |   |   |   |
| Default | 0                | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name             | Description                  |
|------|------------------|------------------------------|
| 15:8 | OTP_IMG_WR_BYTE8 | OTP image byte 8 write field |
| 7:0  | OTP_IMG_WR_BYTE7 | OTP image byte 7 write field |

**7.3.29 OTP\_IMG\_WR5**
**Address: 0x0000 2348**

|         |                   |    |    |    |    |    |   |   |                  |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE10 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE9 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE10 | OTP image byte 10 write field |
| 7:0  | OTP_IMG_WR_BYTE9  | OTP image byte 9 write field  |

**7.3.30 OTP\_IMG\_WR6**
**Address: 0x0000 234A**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE12 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE11 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE12 | OTP image byte 12 write field |
| 7:0  | OTP_IMG_WR_BYTE11 | OTP image byte 11 write field |

**7.3.31 OTP\_IMG\_WR7**
**Address: 0x0000 234C**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE14 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE13 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE14 | OTP image byte 14 write field |
| 7:0  | OTP_IMG_WR_BYTE13 | OTP image byte 14 write field |

**7.3.32 OTP\_IMG\_WR8**
**Address: 0x0000 234E**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE16 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE15 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE16 | OTP image byte 16 write field |
| 7:0  | OTP_IMG_WR_BYTE15 | OTP image byte 15 write field |

**7.3.33 OTP\_IMG\_WR9**
**Address: 0x0000 2350**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE18 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE17 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE18 | OTP image byte 18 write field |
| 7:0  | OTP_IMG_WR_BYTE17 | OTP image byte 17 write field |

**7.3.34 OTP\_IMG\_WR10**
**Address: 0x0000 2352**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE20 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE19 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE20 | OTP image byte 20 write field |
| 7:0  | OTP_IMG_WR_BYTE19 | OTP image byte 19 write field |

**7.3.35 OTP\_IMG\_WR11**
**Address: 0x0000 2354**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE22 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE21 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE22 | OTP image byte 22 write field |
| 7:0  | OTP_IMG_WR_BYTE21 | OTP image byte 21 write field |

**7.3.36 OTP\_IMG\_WR12**
**Address: 0x0000 2356**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE24 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE23 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE24 | OTP image byte 24 write field |
| 7:0  | OTP_IMG_WR_BYTE23 | OTP image byte 23 write field |

**7.3.37 OTP\_IMG\_WR13**
**Address: 0x0000 2358**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE26 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE25 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE26 | OTP image byte 26 write field |
| 7:0  | OTP_IMG_WR_BYTE25 | OTP image byte 25 write field |

**7.3.38 OTP\_IMG\_WR14**
**Address: 0x0000 235A**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE28 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE27 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE28 | OTP image byte 28 write field |
| 7:0  | OTP_IMG_WR_BYTE27 | OTP image byte 27 write field |

**7.3.39 OTP\_IMG\_WR15**
**Address: 0x0000 235C**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE30 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE29 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE30 | OTP image byte 30 write field |
| 7:0  | OTP_IMG_WR_BYTE29 | OTP image byte 29 write field |

**7.3.40 OTP\_IMG\_WR16**
**Address: 0x0000 235E**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE32 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE31 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE32 | OTP image byte 32 write field |
| 7:0  | OTP_IMG_WR_BYTE31 | OTP image byte 31 write field |

**7.3.41 OTP\_IMG\_WR17**
**Address: 0x0000 2360**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE34 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE33 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE34 | OTP image byte 34 write field |
| 7:0  | OTP_IMG_WR_BYTE33 | OTP image byte 33 write field |

**7.3.42 OTP\_IMG\_WR18**
**Address: 0x0000 2362**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE36 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE35 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE36 | OTP image byte 36 write field |
| 7:0  | OTP_IMG_WR_BYTE35 | OTP image byte 35 write field |

**7.3.43 OTP\_IMG\_WR19**
**Address: 0x0000 2364**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE38 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE37 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE38 | OTP image byte 38 write field |
| 7:0  | OTP_IMG_WR_BYTE37 | OTP image byte 37 write field |

**7.3.44 OTP\_IMG\_WR20**
**Address: 0x0000 2366**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE40 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE39 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE40 | OTP image byte 40 write field |
| 7:0  | OTP_IMG_WR_BYTE39 | OTP image byte 39 write field |

**7.3.45 OTP\_IMG\_WR21**
**Address: 0x0000 2368**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE42 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE41 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE42 | OTP image byte 42 write field |
| 7:0  | OTP_IMG_WR_BYTE41 | OTP image byte 41 write field |

**7.3.46 OTP\_IMG\_WR22**
**Address: 0x0000 236A**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE44 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE43 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE44 | OTP image byte 44 write field |
| 7:0  | OTP_IMG_WR_BYTE43 | OTP image byte 43 write field |

**7.3.47 OTP\_IMG\_WR23**
**Address: 0x0000 236C**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE46 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE45 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE46 | OTP image byte 46 write field |
| 7:0  | OTP_IMG_WR_BYTE45 | OTP image byte 45 write field |

**7.3.48 OTP\_IMG\_WR24**
**Address: 0x0000 236E**

|         |                   |    |    |    |    |    |   |   |                   |   |   |   |   |   |   |   |
|---------|-------------------|----|----|----|----|----|---|---|-------------------|---|---|---|---|---|---|---|
| RW      | 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7                 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         | OTP_IMG_WR_BYTE48 |    |    |    |    |    |   |   | OTP_IMG_WR_BYTE47 |   |   |   |   |   |   |   |
| Default | 0                 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name              | Description                   |
|------|-------------------|-------------------------------|
| 15:8 | OTP_IMG_WR_BYTE48 | OTP image byte 48 write field |
| 7:0  | OTP_IMG_WR_BYTE47 | OTP image byte 47 write field |

## 7.4 OTP\_CTRL

### 7.4.1 OTP\_CONTROL1

**Address: 0x0000 2400**

|         |        |   |   |   |   |   |   |             |   |
|---------|--------|---|---|---|---|---|---|-------------|---|
| RW      | 15...8 | 7 | 6 | 5 | 4 | 3 | 2 | 1           | 0 |
|         | —      |   |   |   |   |   |   | OTP_PROG_EN | — |
| Default | 0x04   | 0 | 0 | 0 | 1 | 1 | 0 | 0           | 0 |

| Bits | Name        | Description   |
|------|-------------|---|
| 15:2 | —           | Reserved  |
| 1    | OTP_PROG_EN | OTP programming enable<br>0 = (Default) Disabled (OTP writes ignored)<br>1 = Enabled (OTP writes permitted) |
| 0    | —           | Reserved  |

## 7.5 OTP\_STS

### 7.5.1 OTP\_STS2

**Address: 0x0000 24A8**

|         |    |    |    |    |            |    |   |   |   |   |   |   |   |   |   |   |   |
|---------|----|----|----|----|------------|----|---|---|---|---|---|---|---|---|---|---|---|
| RO      | 15 | 14 | 13 | 12 | 11         | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
|         |    |    |    |    | OTP_IMG_ID |    |   |   |   |   |   |   |   |   |   |   |   |
| Default | 0  | 0  | 0  | 0  | 0          | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits  | Name       | Description   |
|-------|------------|---|
| 15:12 | —          | Reserved  |
| 11:8  | OTP_IMG_ID | Bits [3:1] indicate the ID of the current OTP image. Valid for Production Mode programming only. Note that Bit[0] is not valid.<br>Zero indicates the device has not been programmed in Production Mode.<br>0x0–0x1 = (Default) Blank<br>0x2–0x3 = ID = 1<br>0x4–0x5 = ID = 2<br>0x6–0x7 = ID = 3<br>0x8–0x9 = ID = 4<br>0xA–0xB = ID = 5<br>0xC–0xD = ID = 6<br>0xE–0xF = ID = 7 |
| 7:0   | —          | Reserved  |

### 7.5.2 OTP\_STS3

**Address: 0x0000 24AC**

|         |    |    |    |    |    |    |                 |   |   |   |   |   |   |   |   |   |
|---------|----|----|----|----|----|----|-----------------|---|---|---|---|---|---|---|---|---|
| RO      | 15 | 14 | 13 | 12 | 11 | 10 | 9               | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|         |    |    |    |    |    |    | OTP_IMG_ECC_STS |   |   |   |   |   |   |   |   |   |
| Default | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits  | Name            | Description   |
|-------|-----------------|---|
| 15:10 | —               | Reserved  |
| 9:8   | OTP_IMG_ECC_STS | Indicates the number of errors detected in the OTP payload and parity bits.<br>00 = (Default) No Error, or ECC not run<br>01 = Single Error<br>10 = Double Error<br>11 = Three or more errors |
| 7:0   | —               | Reserved  |

### 7.5.3 OTP\_STS6

**Address: 0x0000 24BC**

|         |        |   |             |   |   |   |   |   |          |
|---------|--------|---|-------------|---|---|---|---|---|----------|
| RO      | 15...8 | 7 | 6           | 5 | 4 | 3 | 2 | 1 | 0        |
|         | —      | — | OTP_IMG_NUM |   |   |   | — | — | OTP_MODE |
| Default | 0x00   | 0 | 0           | 0 | 0 | 0 | 0 | 0 | 0        |

| Bits | Name        | Description  |
|------|-------------|--|
| 15:7 | —           | Reserved   |
| 6:4  | OTP_IMG_NUM | Indicates the number of Production Mode OTP images programmed. A maximum of 7 images can be programmed.<br>000 = (Default) 0 images<br>001 = 1 images<br>...<br>111 = 7 images |

| Bits | Name     | Description   |
|------|----------|---|
| 3:1  | —        | Reserved  |
| 0    | OTP_MODE | Indicates which mode of OTP programming is supported.<br>Note that a blank device supports production or prototype programming. If OTP_MODE=0, check OTP_IMG_NUM to determine if the OTP has already been programmed in Production Mode.<br>If OTP_MODE=0 and OTP_IMG_NUM=0x0, the OTP is blank and supports both programming modes.<br>0 = (Default) Production mode<br>1 = Prototyping mode |

## 8 Thermal Characteristics

Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

| Parameter  | Symbol        | QFN    | Units                       |
|--|---------------|--------|-----------------------------|
| Junction-to-ambient thermal resistance                     | $\theta_{JA}$ | 72.85  | $^{\circ}\text{C}/\text{W}$ |
| Junction-to-board thermal resistance                       | $\theta_{JB}$ | 60.99  | $^{\circ}\text{C}/\text{W}$ |
| Junction-to-case (top) thermal resistance                  | $\theta_{JC}$ | 240.45 | $^{\circ}\text{C}/\text{W}$ |
| Junction-to-board thermal-characterization parameter       | $\Psi_{JB}$   | 52.18  | $^{\circ}\text{C}/\text{W}$ |
| Junction-to-package-top thermal-characterization parameter | $\Psi_{JT}$   | 23.16  | $^{\circ}\text{C}/\text{W}$ |

**Notes:**

- Natural convection at the maximum recommended operating temperature  $T_A$  (see Table 3-1)
- Four-layer, 2s2p PCB as specified by JESD51-9 and JESD51-11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51-12

## 9 Package Dimensions

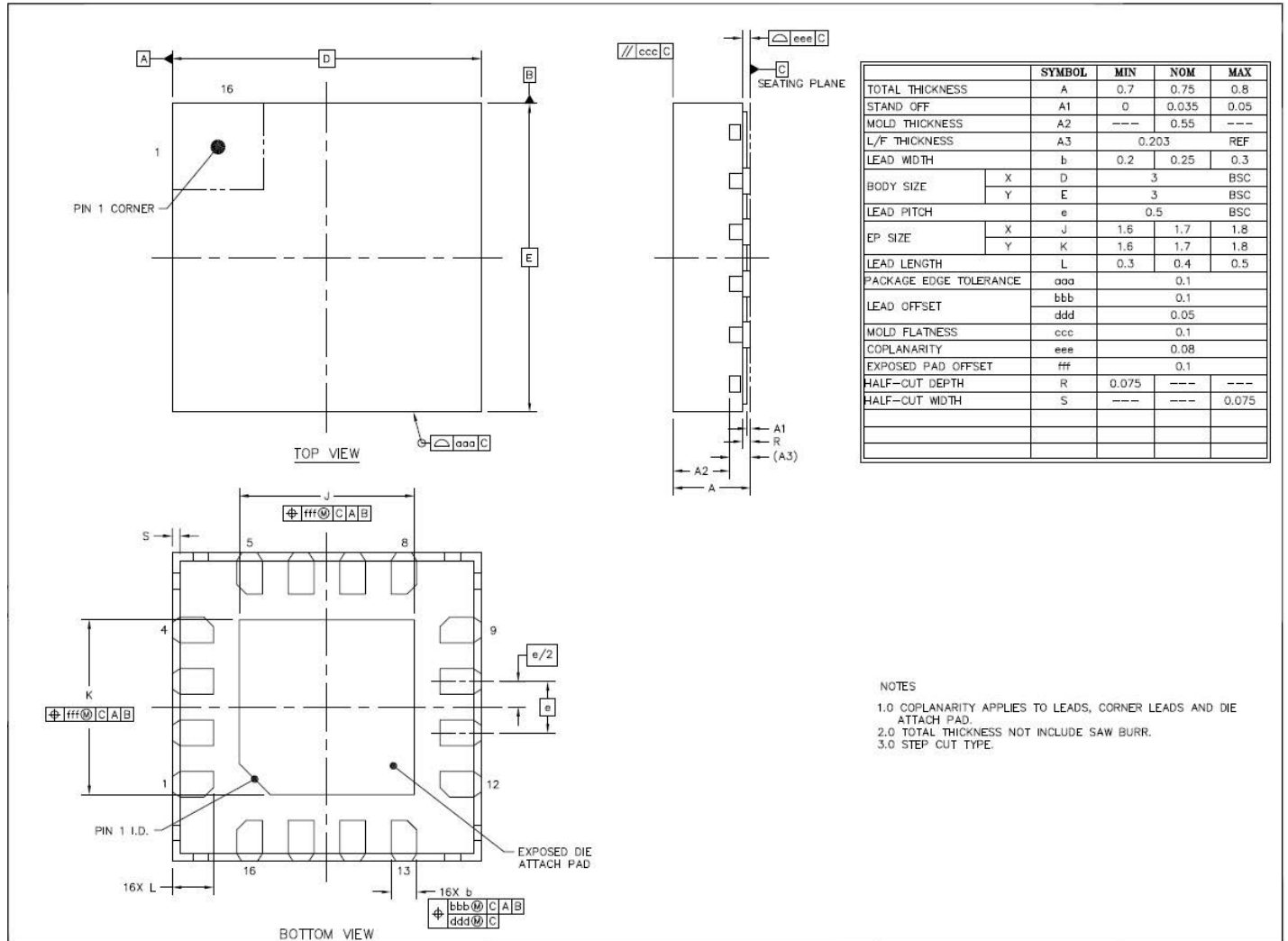
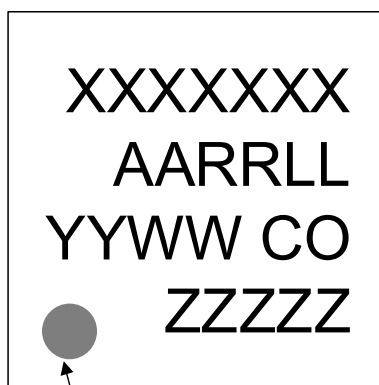


Figure 9-1. QFN Package Dimensions



## 10 Package Marking



Pin 1 Location Indicator

### Top Side Brand

Line 1: Part number  
 Line 2: Package mark  
 Line 3: Package mark date/Country of origin  
 Line 4: Encoded wafer/device ID

### Package Mark Fields

AA = Assembly site code  
 RR = Device revision code  
 LL = Lot sequence code  
 YY = Year of manufacture  
 WW = Work week of manufacture  
 CO = Country of origin

Figure 10-1. Package Marking

## 11 Ordering Information

Table 11-1. Ordering Information

| Product | Description                      | Package    | RoHS Compliant | Grade              | Temperature Range | Container     | Orderable Part Number |
|---------|----------------------------------|------------|----------------|--------------------|-------------------|---------------|-----------------------|
| CS2600  | Clock Synthesizer and Multiplier | 16-pin QFN | Yes            | Commercial         | -40 to +85°C      | Tray          | CS2600-CN             |
| CS2600  | Clock Synthesizer and Multiplier | 16-pin QFN | Yes            | Commercial         | -40 to +85°C      | Tape and Reel | CS2600-CNR            |
| CS2600  | Clock Synthesizer and Multiplier | 16-pin QFN | Yes            | Automotive Grade 2 | -40 to +105°C     | Tray          | CS2600-DN             |
| CS2600  | Clock Synthesizer and Multiplier | 16-pin QFN | Yes            | Automotive Grade 2 | -40 to +105°C     | Tape and Reel | CS2600-DNR            |

## 12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, <http://www.nxp.com>

## 13 Revision History

Table 13-1. Revision History

| Revision       | Change  |
|----------------|---|
| A1<br>JAN 2024 | <ul style="list-style-type: none"> <li>Initial revision.</li> </ul>   |
| A2<br>JUN 2024 | <ul style="list-style-type: none"> <li>Updated CLK_OUT frequency resolution spec (<a href="#">Table 3-4</a>)</li> <li>Noted the FSYNC duty cycle must not exceed 50% (<a href="#">Section 4.5.2</a>)</li> <li>OTP_VDD_EN control bit added (<a href="#">Section 4.7.3.2</a>)</li> <li>Clarified timing-reference options for Hardware Mode (<a href="#">Section 4.9</a>)</li> </ul> |

**Table 13-1. Revision History (Cont.)**

| Revision       | Change   |
|----------------|--|
| A3<br>OCT 2024 | <ul style="list-style-type: none"> <li>• Power-on reset specifications added (<a href="#">Table 3-3</a>)</li> <li>• Specifications and description added for crystal oscillator (<a href="#">Table 3-4</a>, <a href="#">Section 4.2.2</a>, <a href="#">Section 5.1</a>)</li> <li>• Added option to override the automatic REF_CLK source selection (<a href="#">Section 4.2</a>)</li> <li>• Added description of invalid PLL ratio indication (<a href="#">Section 4.3.2</a>, <a href="#">Section 4.4.4</a>)</li> <li>• Clarification of FSYNC duty-cycle limits (<a href="#">Section 4.5.2</a>)</li> <li>• Updated glitchless AUX output switching (<a href="#">Section 4.6</a>)</li> <li>• Noted restriction on writing to AUX1_OUT_DIS and AUX1_OUT_SEL bits (<a href="#">Section 4.6</a>, <a href="#">Section 4.7.3.2</a>)</li> <li>• Clarification of hardware-mode clocking options (<a href="#">Section 4.9</a>)</li> <li>• Added applications information for phase-alignment (<a href="#">Section 5.2</a>)</li> <li>• Added thermal characteristics (<a href="#">Section 8</a>)</li> <li>• Ordering information updated (<a href="#">Section 11</a>)</li> </ul> |
| A4<br>NOV 2024 | <ul style="list-style-type: none"> <li>• Part number and ordering information updated (<a href="#">Table 3-1</a>, <a href="#">Section 11</a>)</li> </ul>   |

**Important:** Please check [www.cirrus.com](http://www.cirrus.com) or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

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